ADVANCED MATERIALS

Silicon Nanowires: A Review on Aspects of their Growth and their Electrical Properties

By *Volker Schmidt,* Joerg V. Wittemann, Stephan Senz,* and *Ulrich Gösele*

This paper summarizes some of the essential aspects of silicon-nanowire growth and of their electrical properties. In the first part, a brief description of the different growth techniques is given, though the general focus of this work is on chemical vapor deposition of silicon nanowires. The advantages and disadvantages of the different catalyst materials for silicon-wire growth are discussed at length. Thereafter, in the second part, three thermodynamic aspects of silicon-wire growth via the vapor–liquid–solid mechanism are presented and discussed. These are the expansion of the base of epitaxially grown Si wires, a stability criterion regarding the surface tension of the catalyst droplet, and the consequences of the Gibbs–Thomson effect for the silicon wire growth velocity. The third part is dedicated to the electrical properties of silicon nanowires. First, different silicon nanowire doping techniques are discussed. Attention is then focused on the diameter dependence of dopant ionization and the influence of interface trap states on the charge carrier density in silicon nanowires. It is concluded by a section on charge carrier mobility and mobility measurements.

1. Introduction

The fiftieth anniversary of silicon-wire research was recently commemorated, a good occasion to take a look back and attempt to review and discuss some of the essential aspects of silicon-wire growth, of the growth thermodynamics, and of the electrical properties of silicon nanowires. The statement of a fiftieth anniversary refers to the publication of Treuting and Arnold of 1957,[1] which, to the best of our knowledge, represents the first publication on Si wire growth. Therein, the authors report on the successful synthesis of silicon whiskers with ⟨111⟩ orientation. At these times, the term whisker was most commonly used in reference to grown filamentary silicon crystals, often times still having macroscopic dimensions (see, e.g., the impressively large wires shown in[2]). In addition to the terms whisker or wire, nanorod is also sometimes used.[3,4]

Throughout this work, the traditional name whisker will not be used, even when referring to the works of old times. Instead, we will use the term silicon wire for filamentary crystals of diameters larger than about hundred nanometers. The term nanowire will be employed in reference to wires of diameters smaller than about hundred nanometers. When general aspects not restricted to a certain size range are discussed, we will use the more general term wire. We will try to stick to this convention, albeit not with uttermost strictness.

Going back to the 1960s, only seven years after the work of Treuting and Arnold was published[1] did research on silicon wires start to really gain momentum, a process clearly catalyzed by the pioneering work of Wagner and Ellis.[5] In this paper, they claimed their famous vapor–liquid–solid (VLS) mechanism of single-crystal growth, which set the basis for a new research field and which until today represents the most common way to synthesize silicon wires. As shown in Figure 1, research on silicon wires basically started with the publication of Wagner and Ellis, flourished for about 10 years, and then ebbed away. Nevertheless, this time was sufficient for the discovery of many of the fundamental aspects of VLS silicon-wire growth.[6]

The second phase in silicon-wire research started in the mid 1990s, when advances in microelectronics triggered a renewed interest in silicon—now nanowire—research. Morales and Lieber[7] managed to synthesize nanowires of truly nanoscopic dimensions and introduced laser ablation as a new method for

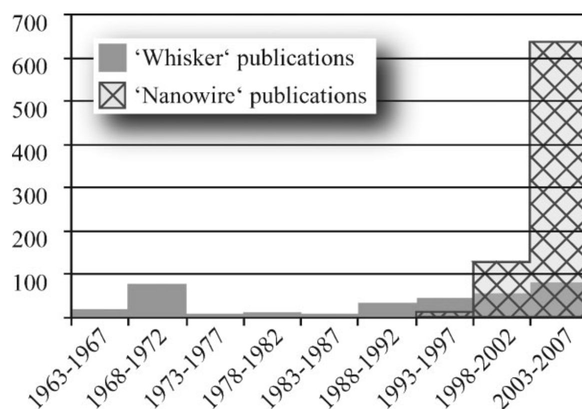

Figure 1. Histogram of the number of silicon "whisker" and "nanowire" publications as a function of the publication date. Source: ISI Web of Knowledge (SM); search date October 9th 2008.

[*] Dr. V. Schmidtz, J. V. Wittemann, Dr. S. Senz, Prof. U. Gösele
Max Planck Institute of Microstructure Physics
Weinberg 2, D–06120 Halle (Germany)
E-mail: vschmidt@mpi-halle.de

DOI: 10.1002/adma.200803754

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim
WILEY InterScience DISCOVER SOMETHING GREAT

Volker Schmidt studied Physics at the Bayerische Julius-Maximilians-Universität Würzburg, Germany, and the State University of New York at Buffalo. He made his PhD at the Max Planck Institute of Microstructure Physics in Halle, Germany, with a dissertation on silicon nanowires growth and properties. Volker Schmidt also worked as a guest scientist at the IBM Zurich research labs in Rüschlikon, Switzerland, and at the materials science department of Stanford University, CA.

Joerg V. Wittemann studied Physics at the Bayerische Julius-Maximilians-Universität Würzburg, Germany and at the University at Albany - State University of New York, where he received a M.Sc. in 2007. After that he joined the Max Planck Institute of Microstructure Physics and began his Ph. D. under the supervision of Prof. U. Gösele. He is currently working on the fabrication and characterization of mechanically strained silicon nanowires.

silicon-nanowire synthesis. Publications on silicon nanowires started to outnumber whisker publications (see Fig. 1), and research on silicon nanowires experienced a remarkable increase in intensity and recognition until today.

With silicon still being the electronics material of choice, it is natural that, aiming at future electronics applications, much of the silicon-nanowire research activities focused on the electrical properties of silicon nanowires, which, of course, necessitates nanowire synthesis. This will also be the focus of this paper, which is aimed at the PhD student starting newly in this field, and tries to provide a short but concise compendium of different aspects of silicon-wire growth and of their electrical properties. We start with the VLS mechanism, because it is really at the heart of silicon-wire research. Following thereupon, a short summary of the various silicon-wire synthesis methods established so far is presented. Concerning the electronics applications, the choice of the catalyst material is essential. Current status of research regarding the various possible catalyst materials is discussed at length. After this more experimental section, focus is shifted to three different thermodynamic effects of VLS silicon-wire growth. These are, first, the expansion at the base of VLS grown wires, because it nicely reflects the interplay between the droplet and the silicon wire. Second, the Nebolsin stability criterion, an insightful wire-growth criterion concerning the value of the droplet surface tension. And third, the Gibbs–Thomson effect and its implications for the silicon-nanowire growth velocity. Last, we will turn our attention to the electrical properties of silicon nanowires and discuss the different doping methods. Then, three effects essential for the conductivity of a silicon nanowire are treated. These are the diameter dependence of the dopant ionization efficiency, the influence of surface traps on the charge-carrier density, also causing a diameter dependence, and the charge-carrier mobility in silicon nanowires.

2. Methods and Materials of Silicon-Wire Growth

2.1. Vapor–Liquid–Solid (VLS) Mechanism

As mentioned, the VLS mechanism, first proposed by Wagner and Ellis[5] in the mid-1960s, is the key mechanism for silicon-wire growth. Their proposed VLS mechanism is based on two observations: that the addition of certain metal impurities is an essential prerequisite for growth of silicon wires in experiments, and that small globules of the impurity are located at the tip of the wire during growth. From this, Wagner and Ellis deduced that the globule at the wire tip must be involved in the growth of the silicon wires by acting "as a preferred sink for the arriving Si atoms or, perhaps more likely, as a catalyst for the chemical process involved".[5] When Au, for example, is deposited on a silicon substrate, and this substrate is then heated to temperatures above about 363 °C, small liquid Au–Si alloy droplets will form on the substrate surface. Exposing such a substrate to a gaseous silicon precursor, such as silicon tetrachloride, $SiCl_4$, or silane, SiH_4, precursor molecules will crack on the surface of the Au–Si alloy droplets, whereupon Si is incorporated into the droplet. The silicon supply from the gas phase causes the droplet to become supersaturated with Si until silicon freezes out at the silicon/droplet interface. The continuation of this process then leads to the growth of a wire with the alloy droplet riding atop the growing wire[5] (see Fig. 2).

The name VLS mechanism refers, of course, to the fact that silicon from the vapor passes through a liquid droplet and finally ends up as a solid. Analogously to the name VLS mechanism, also other growth mechanisms were proposed and accordingly named. Most important in the context of wire growth is the so-called vapor–solid–solid (VSS) mechanism, which comes into

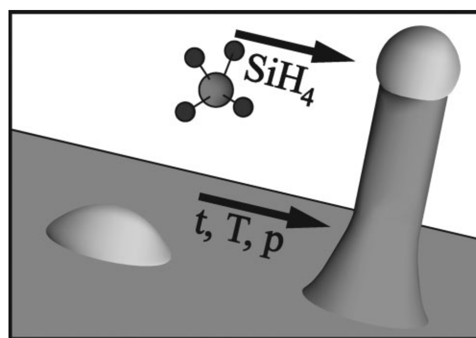

Figure 2. Schematic of the VLS growth mechanism.

WILEY InterScience DISCOVER SOMETHING GREAT
© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

play when wire growth is catalyzed by a solid catalyst particle instead of a liquid catalyst droplet. Whether wire growth proceeds via the VLS or VSS mechanism depends on catalyst material and temperature. Still, it is often difficult to judge and even more difficult to prove which of the two growth modes actually prevailed. In the absence of in situ characterization methods, only the final shape of the catalyst particle can give a hint. It is often noted that in VLS wire growth the radius R of the catalyst droplet exceeds the radius r of the nanowire. One can easily derive that, in equilibrium, $R = r\sqrt{1\Big/\left(1-(\sigma_{ls}/\sigma_l)^2\right)}$,[8] with σ_l and σ_{ls} being the surface tension of the liquid catalyst and the interface tension of the liquid/solid interface, respectively. But the most remarkable feature of the VLS mechanism is that it works well over a large range of sizes, from wires several hundreds of micrometers thick[2] down to nanowires of just a few nanometers in diameter (see, for example, Fig. 8).

2.2. Silicon-Wire Growth Techniques

Before going into the details of wire and nanowire growth, a short summary of the different growth methods is given below.

2.2.1. Chemical Vapor Deposition (CVD)

Like other methods, CVD derives its name from the way the silicon, required for wire growth, is provided. In CVD, a volatile gaseous silicon precursor, such as silane, SiH_4, or silicon tetrachloride, $SiCl_4$, serves as the silicon source. It is transported to the deposition surface at which the precursor reacts, and is cracked into its constituents as depicted in Figure 3a. Originally, CVD was devised for the deposition of high-purity films. Contaminations such as gold particles, however, were found to cause anisotropic growth of silicon, that is, the growth of silicon wires. CVD allows epitaxial growth of silicon wires, with the growth velocity varying from about 10^{-2} to 10^{+3} nm min^{-1},[9,10] depending on temperature and type of Si precursor used. Furthermore, CVD offers broad possibility of modifying the properties of the silicon wires in a controlled fashion (see, for example, Section 4.1).

A variety of derivatives of CVD methods exist. These can be classified by parameters such as the base and operation pressure or the treatment of the precursor. Since silicon is known to oxidize easily if exposed to oxygen at elevated temperatures, it is crucial to reduce the oxygen background pressure in order to be able to epitaxially grow uniform silicon nanowires. In particular, when oxygen-sensitive catalyst materials are used, it turns out to be useful to combine catalyst deposition and nanowire growth in one system, so that growth experiments can be performed without breaking the vacuum in between.[11] In any case, it is useful to lower the base pressure of the CVD reactor down to high or even ultrahigh vacuum, which reduces unwanted contamination and enables growth at lowered temperatures.[12]

The pressures during growth depend mainly upon the gaseous silicon precursor and its cracking probability at the catalyst surface. Growth with disilane, Si_2H_6, for example, can—but must not—be carried out at extremely low partial pressures of around 10^{-6} mbar (1 bar $= 10^5$ Pa). These low growth pressures allow the combination of CVD with transmission

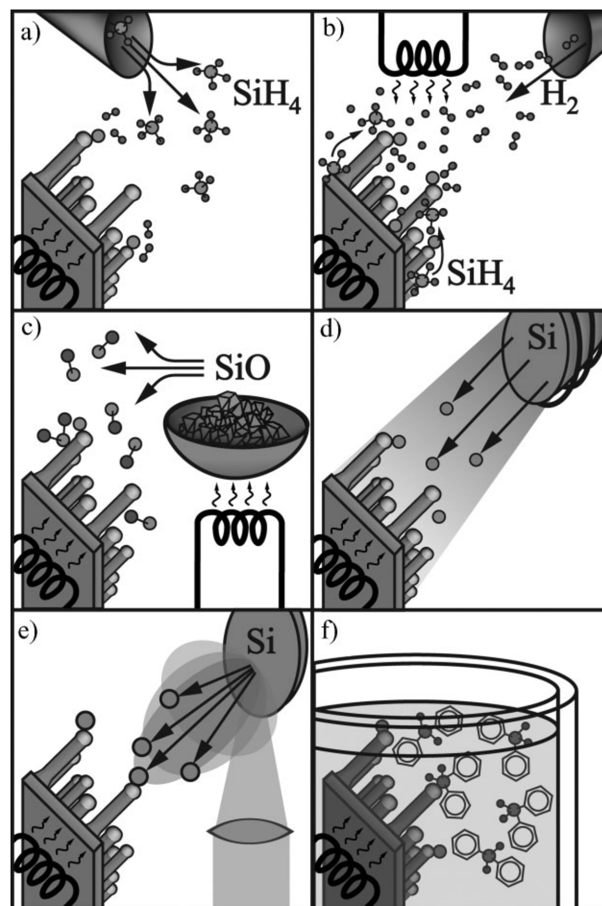

Figure 3. Schematics of experimental setups for silicon nanowire growth. a) CVD, b) annealing in reactive atmosphere, c) evaporation of SiO, d) MBE, e) laser ablation, and f) solution-based growth.

electron microscopy (TEM), enabling in situ observation of the nanowire growth.[13] In contrast to that, silane partial pressures required for wire growth are about five orders of magnitude higher.

By modifying the precursor before reacting with the sample surface, the temperature budget of the substrate can be lowered. In cases where the thermal load is critical or where a high supersaturation of the droplet is necessary, nanowire growth can be enhanced using plasma-enhanced CVD (PECVD).[14–16]

Another advantage of CVD as a bottom-up synthesis method is its variability concerning the intended wire size. Wire diameters range from below 10 nm[17] up to several hundred micrometers.[5] Since surface diffusion only plays a minor role in CVD, the length of the wires can also be tuned accordingly by simply extending or decreasing the growth time. Thus, to summarize, a large range of length and diameter configurations can be fabricated.[18] With CVD not only the wire size but also its properties can be modified. CVD offers the opportunity of a controlled doping by intentionally offering additional doping precursors. By switching the doping precursor, doping profiles in axial direction can be created.[19–22]

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

WILEY InterScience DISCOVER SOMETHING GREAT

One of the major problems of silicon nanowires grown by CVD is that they exhibit a certain variation of the growth direction, especially for diameters smaller than about 50 nm.[23] This obstacle, however, can be overcome when the nanowires are grown in a template, such as anodic aluminum oxide (AAO).[24–26] Here, the catalyst material is deposited into the pores of an AAO membrane, so that wire growth is confined to the AAO pore. Thereby, the wire is forced to grow along the pore direction. In this way, epitaxial ⟨100⟩ oriented nanowires—an orientation not favored by free-standing nanowires—can be achieved. Subsequent to growth, the template can be removed with phosphoric acid, leaving just the nanowires standing on the substrate.

2.2.2. Annealing in Reactive Atmosphere

Already pioneered in the early 1960s, a method to synthesize silicon whiskers was to expose a crystalline silicon, contaminated with certain metal impurities to reactive gases like hydrogen, iodine, or bromine, and heat it up to about 900 °C.[27–29] At such temperatures, the gases can react with the solid silicon, locally generating silicon compounds like SiH_4,[30] SiI_2, or $SiBr_2$.[31] The metal-droplet contamination acts as catalyst and growth proceeds as in conventional CVD. The main advantage of this method is clearly its technical simplicity, which is presumably the reason why it was used in the early works on silicon-wire growth. In some sense, this method can be seen as the predecessor of wire growth by conventional CVD. As schematically indicated in Figure 3b, a modification of this method, used nowadays, is hot-filament CVD.[32]

2.2.3. Evaporation of SiO

A cost-effective method to produce silicon nanowires on a large scale is to evaporate solid silicon monoxide, SiO (see Fig. 3c). A two-zone tube furnace connected to an inert gas supply and small amounts of SiO granulate are the basic requirements for the synthesis of silicon nanowires. Crucial for growth is a temperature gradient from about 1350 to 900 °C along the tube of the furnace. SiO is evaporated at the hotter end of the tube, flows with the gas stream to the cooler part, where it undergoes a disproportionation reaction into Si and SiO_2, thereby forming the nanowires.[33]

In principle, two different growth methods are possible: growth with and without metal catalyst. Growth assisted by the presence of a metal catalyst is relatively rapid.[34] Consistent with the concept of VLS growth, the diameters are determined by the size of the catalyst particle, although the interplay between the nanowire and the catalyst droplet seems to be more complex compared to normal CVD growth. As a consequence of the disproportionation reaction, the diameter ratio between crystalline core and amorphous shell remains approximately constant.[35] The second growth mode, metal-catalyst-free growth, has been originally proposed for growth via laser ablation,[36] where it was observed that nanowires can be catalyzed by silicon dioxide.[37] Remarkable about this oxide-assisted growth (OAG) is that SiO_2-containing targets clearly raise the yield of the final amount of silicon nanowires compared to pure silicon targets or mixed silicon–metal targets.[36] By carrying out the growth process over several hours, one can obtain millimeter-long crystalline silicon nanowires with varying diameters from about 5 to 100 nm, covered by an amorphous shell of up to several 10 nm.[38–40]

2.2.4. Molecular Beam Epitaxy (MBE)

In MBE, a solid high-purity silicon source is heated until Si starts to evaporate. Figure 3d schematically depicts an MBE setup. A directional gaseous beam of silicon atoms is aimed at the substrate, on which the atoms adsorb and crystallize. To reduce contamination, the base pressure of an MBE system is usually kept at ultrahigh vacuum, allowing to monitor the growth using reflection high-energy electron diffraction[41] or other surface-sensitive examination methods. Similar to CVD, MBE was initially designed for epitaxial layer-by-layer deposition only. Yet, metal contamination was also found to cause silicon-wire growth in this case. Differing from CVD, no precursor gas is cracked at the surface of the liquid metal–silicon alloy. Therefore, the latter cannot be treated as a classical catalyst anymore. In MBE, two silicon fluxes govern wire growth. First, the direct flux of silicon from the silicon source; and second, the flux of diffusing silicon adatoms from the silicon substrate surface. The nanowires produced by MBE—usually grown on Si(111) substrates—are epitaxial and ⟨111⟩ oriented. MBE offers excellent controllability in terms of the incoming flux, such that doped wires[42] or heterostructures[43] can be grown by switching between evaporation sources. One disadvantage of MBE, however, is that the method is limited with respect to the minimally possible Si-nanowire diameter. Only nanowires with diameters greater than about 40 nm can be obtained,[41,44] which seems to be a consequence of the Gibbs–Thomson effect, and the fact that only small Si supersaturations are achievable by MBE. Another disadvantage of MBE is the low nanowire growth velocity of a just a few nanometers per minute.[44]

2.2.5. Laser Ablation

The silicon nanowires produced by laser ablation differ in many aspects from the MBE grown whiskers. One can easily obtain large quantities of ultrathin nanowires with high aspect ratios.[45,46] As schematically displayed in Figure 3e, a high-power pulsed laser ablates material from a mixed Si–catalyst target, which is placed in a tube furnace held at high temperatures and purged with an inert gas. The silicon material ablated from the target cools by colliding with inert-gas molecules, and the atoms condense to liquid nanodroplets with the same composition as the target.[7] Thus, these nanoparticles contain both Si and the catalyst material. According to the VLS mechanism, silicon nanowires start to grow once the catalyst gets supersaturated with silicon and proceeds as long as the catalyst nanoparticles remain liquid. The advantages of laser-ablated nanowire production are manifold. First, there is no need for a substrate. Second, the composition of the resulting nanowires can be varied by changing the composition of the laser target. By adding, for example, SiO_2 to the target, single-crystalline silicon nanowires with varied amorphous SiO_x shell thicknesses can be obtained in a single processing step,[47] with silicon-core diameters as low as 5 nm and varying shell thicknesses of about 10 nm. Due to the high growth temperatures, catalyst metals such as Fe, possessing a high eutectic temperature, can be used. The resulting nanowire growth velocities are typically of the order of micrometers per

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

minute.[7,45] The radii of the nanowires not only depend on the type of metal catalysts used but also on the gases that are streamed through the furnace, such as H_2, He, or N_2.[48]

2.2.6. Solution-Based Techniques

Wire growth can not only take place in gaseous environments, but also in liquid media. These solution-based growth techniques are the methods of choice for high-yield silicon-nanowire production. One method utilizes highly pressurized supercritical organic fluids enriched with a liquid silicon precursor, such as diphenylsilane, and metal catalyst particles, as indicated in Figure 3f. At reaction temperatures above the metal–silicon eutectic, the silicon precursor decomposes and silicon forms an alloy with gold. Analogously to the VLS mechanism, the alloy droplet in this supercritical–fluid–liquid–solid (SFLS) method starts to precipitate a silicon nanowire once the alloy gets supersaturated with silicon.[49–51] Crystalline nanowires with diameters as low as 5 nm and several micrometers in length have been fabricated using this approach. Similar to the VSS mechanism, silicon-nanowire growth via a solid catalyst particle has also been demonstrated for the solution-based method. Micrometer-long nanowires were synthesized at a temperature of merely 500 °C using copper particles as catalysts.[52] Another high-yield silicon-nanowire production method is the so-called solution–liquid–solid (SLS) method. Here, the growth environment is not a supercritical liquid, but an organic solvent at atmospheric pressure, and the production of micrometer-long crystalline wires, 25 nm in diameter, has been demonstrated.[53] The SLS method probably represents the most-cost-effective nanowire-production method, as it can be realized without high-priced equipment.

2.2.7. Top-down Fabrication Methods

In addition to the different bottom-up fabrication methods discussed above, several attractive top-down approaches for the fabrication of single crystalline silicon nanowires exist. Due to the processing-related differences, one should distinguish between the fabrication of horizontal nanowires, that is, nanowires lying in the substrate plane, on the one hand, and the fabrication of vertical nanowires, that is, nanowires oriented more or less perpendicular to the substrate, on the other. Horizontal silicon nanowires are mostly fabricated from either silicon-on-insulator (SOI) wafers[54–56] or bulk silicon wafers[57,58] using a sequence of lithography and etching steps, often employing electron-beam lithography and reactive ion etching. This shall be plainly stated here without going into the details of the processing schemes, which would be beyond the scope of this paper. The interested reader is kindly referred to the excellent articles of Singh et al.[59] and Suk et al.[57,58] and the references therein. In most cases, horizontal nanowire processing is finalized by an oxidation step, which also serves to reduce the silicon nanowire diameter. In this way, diameters well below 10 nm have been achieved in the past.[58,59] No further thinning of the nanowires is necessary in the so-called superlattice nanowire pattern-transfer (SNAP) technique.[60] In this approach a differentially etched GaAs/AlGaAs superlattice is used as a stamp to transfer thin metal lines onto the substrate, which can then be used for further processing.

Using standard silicon technology, vertical silicon nanowires can also be produced. Often, reactive-ion etching is used to etch vertical silicon nanowires out of a silicon wafer. The diameter of the nanowires is defined by a lithography step preceded by reactive ion etching. A variety of different nanostructuring methods, such as electron-beam lithography,[61] nanosphere lithography,[62] nanoimprint lithography,[63] or block-copolymers[3] have been employed for this purpose. As an alternative to reactive-ion etching, the so-called metal-assisted etching of silicon attracted some attention recently. In this approach Si is wet-chemically etched, with the Si dissolution reaction being catalyzed by the presence of a noble metal that is added as a salt to the etching solution.[64–66] Alternatively, also a continuous but perforated noble-metal film can be used. During etching, this perforated metal film will etch down into the silicon producing vertical silicon nanowires at the locations of the holes in the metal film.[67,68]

2.2.8. Summary

To summarize, the various growth methods are quite distinct in their characteristics, and the question of which method suits best depends, to a large extent, on the application. In particular, one should distinguish here between approaches for the in-place fabrication of silicon nanowires, that is, the synthesis of nanowires directly at a specific position on the substrate, and approaches where nanowire fabrication—irrespective of position—is performed in a first step, potentially followed by a subsequent assembly step. Concerning the former, the in-place fabrication of silicon nanowires, one must conclude that so far none of the bottom-up synthetic methods can compete with the top-down fabrication methods in terms of controllability, reliability, and size variability. The one that comes closest is presumably CVD, as it allows for an epitaxial growth on silicon substrates at specific positions, and additionally offers great versatility concerning process conditions, nanowire dimensions, and properties. MBE, though combining epitaxial growth with a good controllability of composition, lacks the variability of CVD concerning nanowire diameters and aspect ratios. Having the synthesis of non-substrate-bound nanowires in mind, laser ablation and solution-based growth techniques appear as the methods of choice, since laser ablation combines a good controllability and variability of the nanowire composition with excellent nanowire quality and reasonable yield and solution-based growth techniques offer a high nanowire yield, which makes this approach especially attractive for large-scale nanowire production.

2.3. Gold as Catalyst

Since the early publications of Wagner and Ellis,[5] Au has been the catalyst material of choice for growing Si wires. It is still, without doubt, the most frequently used catalyst material. Of course, one could simply be satisfied by knowing that Au is the catalyst material that works best, or at least easiest, and just use it for Si nanowire growth; but in this case the question of why gold is such a favorable catalyst remains unanswered. We will see in the following that it is indeed instructive to take a closer look at the Au–Si system, because one can identify general criteria that can also be applied to the use of other catalyst materials.

 © 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim WILEY InterScience DISCOVER SOMETHING GREAT

ADVANCED MATERIALS

First, we will present some advantages that speak in favor of using Au from a purely practical point of view. One is availability. Gold is one of the standard metals used for electrical contacts. Evaporation systems equipped with Au can be found in most semiconductor research institutes. Thus, depositing a thin layer of Au onto a sample substrate usually does not impose a major obstacle. Alternatively, one could use colloid nanoparticles, which in case of Au are commercially available with diameters ranging from 2 to 250 nm (see, for example, ref. [69]). Another advantage of Au is related to its most prominent property, namely its high chemical stability. Although seemingly trivial, this is a highly important issue for the handling of samples. In particular, when the pregrowth processing of a sample is intended, it is advantageous to use a catalyst material that does not oxidize easily in air. Moreover, the high chemical stability of Au reduces the technical requirements on the growth system, especially with regard to the maximum tolerable oxygen background pressure. Furthermore, the safety requirements for the use of Au are low, as Au is not toxic.

A schematic of the Au–Si binary phase diagram (PD) is shown in Figure 4a. The Au–Si PD is of the simple eutectic type. Its dominant feature is a eutectic point at about 19 at.% Si and 363 °C, which signifies a remarkably strong reduction of the melting temperature compared to the melting points of pure Au or pure Si. Heating a Au-covered Si sample to a temperature higher than the eutectic point will result in the formation of a liquid Au–Si alloy. This process is accompanied by a dewetting, which means that instead of a homogeneous layer, a distribution of small Au–Si droplets will form. By annealing further, the larger droplets will grow at the expense of the smaller ones, corresponding to a continuous increase in the mean droplet size with time. This phenomenon is commonly known as Ostwald ripening[70] (for a theoretical treatment, see refs. [71–74]).

The phase within the V-shaped region of the PD of Figure 4a is the liquid phase. The actual composition of the liquid is determined by the amount of Si supplied. Considering Au–Si alloy droplets on a Si substrate, Si is abundant. Consequently, the Si concentration in such Au–Si droplets corresponds to a composition as given by the Si-rich liquidus line, that is, the phase boundary on the right-hand side (rhs) of the liquid phase. By exposing the sample at these elevated temperatures to a Si precursor such as, for example, silane, SiH_4, silane molecules will crack at the surface of the droplet, and additional Si will be incorporated. This additional Si supply will then cause an increase in the Si concentration in the droplet beyond the equilibrium composition. Considering the Au–Si PD, this means that the Au–Si droplet system will be located slightly to the right of the liquidus line. In an attempt to re-establish equilibrium, the droplet precipitates a solid with higher Si concentration, whose composition is given by the next phase boundary on its Si rich side. In the Au–Si case, this happens to be pure Si. By continuously supplying Si, one can synthesize Si wires or nanowires via this non-equilibrium process.

Generally speaking, Si-wire growth requires a non-horizontal phase boundary in the corresponding metal–Si PD. By increasing the Si pressure, one can then push the droplet system over this phase boundary to enforce the precipitation of a Si-rich solid. The phase boundary has to be neighboring the pure Si side of the PD to ensure that the precipitated solid is pure Si. In case of the VLS growth mode, this phase boundary corresponds to the liquidus line, as indicated in Figure 4a or c; but this is not a necessity. Considering VSS Si-wire growth, that is, growth via a solid catalyst particle, the phase boundary, where the precipitation of Si takes place, can either be a boundary that limits the solubility of Si in the catalyst metal itself (see, for example, the Al pocket on the left hand side (lhs) of Fig. 4b), or it can as well be the boundary of a silicide phase, like the $TiSi_2$ phase marked by a vertical line in Figure 4d. According to the aforementioned statement that the phase boundary at which Si wire growth takes place has to neighbor pure Si, one can expect most Si-rich silicide to be present during wire growth. We will see later on that this is consistent with experimental observation.

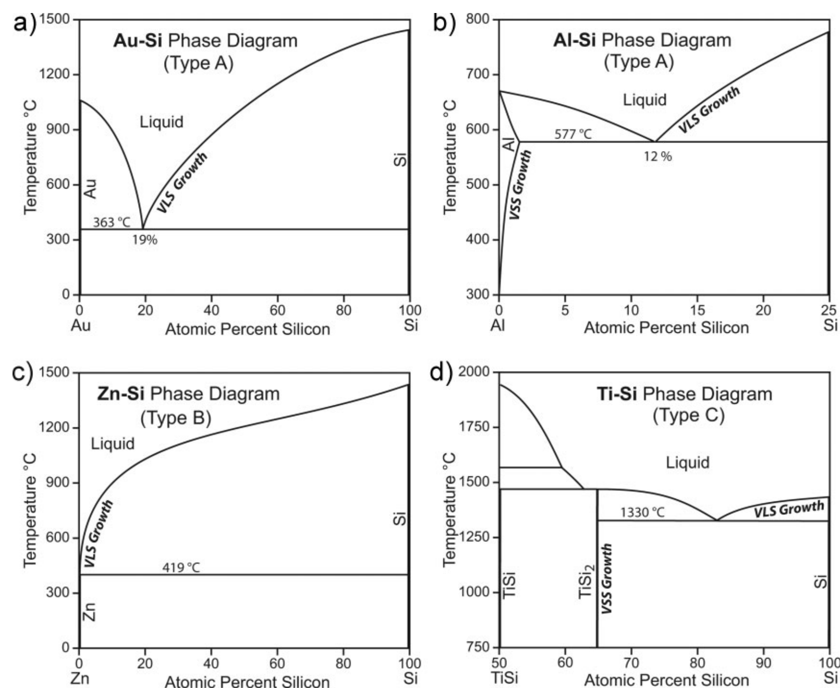

Figure 4. Schematics of various metal–Si PDs or parts of the metal–Si PDs: a) Au–Si, b) Al–Si, c) Zn–Si, d) Ti–Si; after.[108] The types refer to the classification shown in Figure 6.

An important feature of the Au–Si binary PD (see Fig. 4a) is its relatively high Si concentration of 19 at.% at the eutectic point. This high solubility at the eutectic temperature indicates that the energetic costs of dissolving Si in a Au–Si alloy must be low, since Si apparently likes to mix with Au. Consequently, the energetic costs per Si atom of increasing the Si concentration beyond its equilibrium value should also be comparably low (also indicated by the low steepness of the liquidus). Thus, the Si pressure required to achieve a certain increase in the Si concentration beyond its equilibrium value should be lower for

WILEY InterScience DISCOVER SOMETHING GREAT
© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

metals with a high Si solubility at the eutectic point. According to this argument, Au is a well-suited catalyst, because one can work at relatively low Si-precursor pressures. For completeness, it should be noted that the large solubility of Si at the eutectic point can also turn into a disadvantage, if one aims at the growth of axial Si–Ge heterostructures with sharp interfaces.

Another important property of Au that must not be forgotten is its conveniently low vapor pressure, even at high temperatures. The vapor pressure of Au is smaller than 10^{-8} mbar for temperatures below about 800 °C. Under usual Si-wire growth conditions, an unwanted evaporation of the catalyst material is therefore not critical. We will see later on that there are indeed several potential catalyst materials that can be excluded just because of their high vapor pressure. One aspect that has not been addressed concerns the surface tension of a Au–Si liquid. We will see in Section 3.2 that a certain minimum value of the droplet surface tension is required in order to have a stable droplet–nanowire system. This criterion is well met by a Au–Si alloy.

To summarize this part briefly, the advantages that render Au such a favorable catalyst material are that Au is nontoxic, chemically inert, and easily available, that it possesses a eutectic point at a low temperature but high Si solubility, that Au has a low vapor pressure at elevated temperatures, and that the Au–Si liquid alloy has a high-enough surface tension. Unfortunately, this bundle of advantages is balanced by one serious drawback. This is that Au, which is a known impurity in nanowires,[75–77] is considered incompatible with industrial electronic production standards, as will be discussed in the following subsection.

2.4. Alternative Catalyst Materials

In recent years, numerous research efforts have focused on identifying an alternative, that is, non-Au, catalyst material for Si-wire growth. This renewed interest arouse partly because Au is deemed incompatible with complementary metal-oxide-semiconductor (CMOS) production standards. The reason why Au is usually thought of as being incompatible is that Au is known to create deep level defects in Si (see Fig. 5). Impurities in a semiconductor can affect the charge-carrier lifetime by acting as centers for charge-carrier recombination. The maximally possible recombination rate associated with a certain impurity depends on the energetic positioning of the impurity level within the bandgap. To be more precise, it critically depends on the energetic difference between the impurity level and the center of the band gap—the closer the impurities level is to the band-gap middle, the more efficient it is as a recombination center. Therefore, the incorporation of impurities with levels close to band-gap middle, the so-called deep levels, is avoided as far as possible. Concerning Au, the problem is further augmented by its high chemical stability, which renders cleaning Au-contaminated samples, or even more important, Au contaminated equipment, difficult.

Figure 5 shows the impurity levels of various potential catalyst materials as a function of the corresponding minimum temperature required for a VLS growth. These are the metals

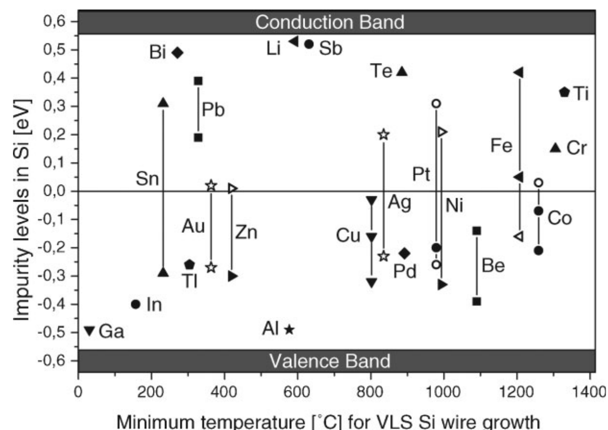

Figure 5. Ionization energies of various impurities in Si (after Sze[142]) given with respect to the middle of the bandgap (assuming a bandgap of Si of 1.12 eV) as a function of the minimum temperature necessary for VLS growth. In case an impurity possesses two or more levels, these are shown connected by a line. Levels above the bandgap middle that are marked with solid symbols are donor levels, whereas open symbols indicate acceptor levels. Analogously, full symbols below the bandgap middle are acceptor levels, whereas open symbols are donor levels.

with impurity levels close to the valence or conduction bands, and which therefore would cause a doping of Si: p-doping for In, Ga, Al; n-doping for Bi, Li, Sb, Te. Depending on whether a doping of the Si wires is intended or not, these materials could be attractive candidates for Si-wire growth. Second, there are those that have levels close to the band-gap middle, such as like Au, Zn, Cu, Fe, Cr, Pb, or Co. If both, high doping and active charge-carrier recombination, are to be avoided, Sn, Tl, Ag, Pt, Pd, Ni could possibly be attractive catalyst materials, if, of course, Si wires can actually be synthesized using these catalysts.

To see whether this is the case, the literature reported on the use of non-Au catalysts can be searched. Here is the hopefully complete list of catalyst materials for which successful Si-wire synthesis has been reported: Ag,[2,5,8,10,28,78,79] Al,[8,11,16,80–84] Bi,[85] Cd,[28] Co,[36] Cu,[2,5,8,10,28,75,78,86–88] Dy,[89] Fe,[7,36,89–92] Ga,[8,15,84,93,94] Gd,[28] In,[8,16,85,93,95] Mg,[28] Mn,[28] Ni,[2,5,6,8,10,28,29,36,78,96–98] Os,[28] Pb,[85] Pd,[5,6,8,13,28,78] Pt,[2,5,6,8,10,99–101] Te,[85] Ti,[102–104] and Zn.[8,85,105,106] The number of possible catalyst material is actually not so small. In order to discuss the differences and similarities between the various catalysts in a concise manner, it is helpful to classify them with respect to the characteristics of the corresponding metal–Si binary PD.

We adopt the following classification scheme, shown in Figure 6. Type A catalysts have a simple eutectic PD, which means that the PD is dominated by a single eutectic point. This eutectic point is located at a Si concentration greater than 10 at.%. Furthermore, type A catalysts are characterized by the absence of any metal–silicide phases. Type B catalysts are also characterized by a dominant eutectic point and the absence of silicide phases. Yet, in contrast to type A catalysts, the eutectic point is located at very low Si concentrations, smaller than 1 at.%. Type C catalysts are characterized by the presence of one or more silicide phases. In addition, their eutectic points can all be found at temperatures >800 °C.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

WILEY InterScience® DISCOVER SOMETHING GREAT

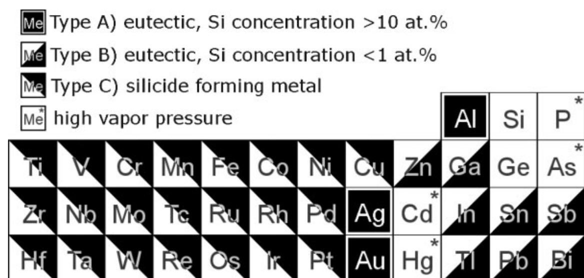

Figure 6. Periodic table with potential catalyst metals classified according to their PD.[108] Type A) PD dominated by a eutectic point at a Si concentration >10%; no metal–silicide phase present. Type B) PD dominated by a eutectic point at a Si concentration <1%; no metal–silicide phases present. Type C) PD shows the existence of one or more metal–silicide phase; eutectic points are located at temperatures above 800 °C. Elements marked with a star * have a vapor pressure of more than 0.01 mbar at 300 °C.

2.4.1. Type A Catalysts

Among the various catalyst materials, Al is the one whose PD, shown in Figure 4b, shows the closest similarity with the Au–Si one. The eutectic point of the Al–Si system is located at higher temperatures (577 °C) and slightly lower Si concentrations (12 at.%) compared to Au, but otherwise the two PDs are very similar. It is therefore not too astonishing that VLS growth using Al indeed works. Osada et al.[80] demonstrated Al-catalyzed VLS growth of well-crystalline Si wires by means of a CVD process using silane and temperatures between 580 and 700 °C. Also Whang et al.[81–83] studied the Al mediated Si nanowire CVD synthesis, using silane as precursor. They claim to have grown Si nanowires via the VLS mechanism at 540 °C without substantiating their claim, although the growth temperature used was almost 40 K below the Al–Si eutectic temperature. Thus, one may doubt whether VLS growth indeed occurred; in particular, in view of the fact that an apparent VSS growth of Si nanowires using Al as catalyst has been demonstrated.[11] In a process similar to that of Whang et al. (also CVD with silane as precursor and Al as catalyst), Wang et al.[11] demonstrated the synthesis of nicely regular, single-crystalline Si nanowires grown epitaxially on Si (111) substrates at a growth temperature between 430 and 490 °C, well below the Al–Si eutectic point. From this, Wang et al.[11] concluded that Si nanowires grew via the VSS mechanism. They point out that VSS growth using Al is related to a characteristic feature of the Al–Si PD—namely the pocket on the lhs of Figure 4b. This pocket signifies that a non-negligible amount of Si can be dissolved in solid Al at elevated temperatures (about 1 at.% Si at 500 °C). The phase boundary that limits the solubility of Si in solid Al is neighboring the pure Si side of the PD (there is no other phase in between). As discussed before, by exerting a certain Si pressure, this phase boundary can be used to induce a phase separation, that is, the precipitation of Si leading to wire growth.

Compared to the VLS growth of Si wires, synthesis via solid Al particles brings the advantage that the solubility of Si in the catalyst particle is about one order of magnitude smaller. This low solubility might turn out to be a useful feature if one aims, for example, at the fabrication of axial Si/Ge heterostructures. Due to the low Si solubility in solid Al, sharp transitions between Si and Ge should be achievable. Concerning the electrical properties, the position of the impurity level shown in Figure 5 implies that Al will act as a p-type dopant. Whether p-type doping is an advantage or disadvantage depends on the application, but the ability to directly synthesize highly p-doped wires is at least an interesting feature. A comparison with solid-phase epitaxy experiments[107] shows that one can expect an Al dopant concentration between 10^{18} and $10^{19}\,cm^{-3}$. Finally, it should be remarked that oxidation of the catalyst particle seems to be a crucial issue when Al is used as catalyst. In order to be able to grow Si wires with Al, care has to be taken with respect to the oxygen background pressure in the growth system.

The other non-gold type A catalyst is silver. The Ag–Si system possesses a single eutectic point at 11 at.% Si and 835 °C. Consequently, rather high temperatures are required for a VLS growth of Si wires. Wagner and Ellis[2] reported on VLS-grown single-crystalline Si wires using Ag as catalyst, synthesized in a CVD process with $SiCl_4$ as precursor at 950–1050 °C. The possibility of VLS growth under such conditions has been confirmed by Nebol'sin et al.,[10] who grew Si wires at a growth rate of about 1.5 $\mu m\,s^{-1}$ in a CVD process at 1197 °C, also using $SiCl_4$ as precursor. Concerning a VSS growth of Si wires with the help of Ag as catalyst, Tatsumi et al.[79] claim to have synthesized amorphous Si wires in a silane CVD process at a temperature of 650 °C, well below the eutectic temperature. This at first seems surprising, because the Ag–Si PD as given in ref. [108] does not indicate any Si solubility in solid Ag. Yet, a certain solubility of Si in the catalyst particle seems to be necessary for wire growth. The riddle, however, was solved by a recent analysis of the PD,[109] which revealed that the solid solubility of Si in Ag is about 0.9 at.% at the eutectic temperature, and 0.2 at.% at 650 °C. Hence, the Ag–Si PD strongly resembles the Al–Si PD shown schematically in Figure 4b, but with an eutectic point at higher temperatures and the Ag pocket less pronounced than the Al pocket on the lhs of Figure 4b. Analogously to VSS Si-nanowire growth with Al, VSS growth via solid Ag particle seems to be promising, in particular as the impurity levels of Ag (see Fig. 5) are neither very close to the band-gap center nor to the band-gap edges.

2.4.2. Type B Catalysts

The characteristic feature of type B catalysts is a eutectic point at very low Si concentrations. Let us first consider the transition metals Zn and Cd. The Zn–Si binary PD, schematically reproduced in Figure 4c, is dominated by a eutectic point at 420 °C and a 0.02 at.% Si. Despite its significant vapor pressure, of about 0.2 mbar at 420 °C, Zn has been shown to be an effective catalyst material. Chung et al. and Yu et al.[105,106] demonstrated VLS Si-nanowire growth by means of a CVD process using silane at a partial pressure of 6.7 mbar and a temperature between 440 and 500 °C. They obtained Si nanowires with diameters between 15 and 35 nm, and observed both $\langle 111 \rangle$ and $\langle 211 \rangle$ oriented nanowires with the $\langle 211 \rangle$ being nearly defect-free.[106] Concerning the electronic properties (see Fig. 5), one must conclude that the impurity levels of Zn in Si are as unfortunate as those of Au. Overall, it seems there is little to gain by switching from Au to Zn, except that a Zn contamination could possibly be more easily removed (by annealing) than Au contamination.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

On the use of Cd as catalyst, only little is known, except for the remark that "cadmium promoted whisker growth when the source material was arsenic-doped silicon".[28] Judging from the PD (eutectic point at 321 °C and 0.14 at.% Si), which resembles that of Zn, Si-wire growth via the VLS mechanism could be possible, if one was able to prevent complete evaporation of Cd during growth. Similarly to Zn, Cd possesses a very high vapor pressure, of more than 1 mbar, at 321 °C. This high vapor pressure severely limits the usability of Cd as catalyst material.

Much more interesting from an electronics point of view is the use of Ga or In as catalyst, because In and Ga would cause a strong p-type doping of the wires (see Fig. 5). Also in terms of vapor pressure, In and Ga are much more favorable than Zn or Cd. At 500 °C, the vapor pressure of In is below 10^{-7} mbar and the vapor pressure of Ga below 10^{-10} mbar. Concerning the PDs, Ga and In show great similarities. The Si concentrations at the eutectic points of In or Ga are both very small (<0.01 at.%). Also the eutectic temperatures of Ga (30 °C) and In (156 °C) do not differ too much, in the sense that any reasonable CVD growth temperature will be way above the eutectic temperature. So one can expect Si-wire growth experiments using In or Ga to produce similar results, an assumption that has been experimentally confirmed by Givargizov and Sheftal,[93] who managed to synthesize conical Si wires using In and Ga in a high-temperature (900–1050 °C) CVD process using $SiCl_4$. The conical shape is attributed to the incorporation and/or evaporation of the catalyst material.[93] More recently, Iacopi et al.[16,95] using In, and Sharma and Sunkara[15] using Ga, demonstrated the synthesis of Si nanowires of good crystallinity. Both used PECVD with silane as Si precursor and temperatures between 500 and 600 °C to produce Si nanowires. Concerning the other, type C, catalysts, that is, Tl, Sn, Pb, Sb, and Bi, there exists only one—unfortunately not very detailed—publication by Miyamoto and Hirata,[85] in which the growth of amorphous Si fibers at temperatures between 500 and 600 °C with Bi and Pb as catalysts is mentioned. Since the eutectic temperatures of Pb and Bi are at 328 and 271 °C, respectively, VLS growth seems possible. However, according to Nebol'sin et al.[8] the surface tensions of liquid Sn, Pb, Sb, or Bi are in a range that does not allow stable wire growth. This surface-tension criterion will be discussed in detail in Section 3.2. Just considering the electronic properties in Si, the use Bi, Tl, and Sn as catalyst seems attractive—Bi when doped, Tl and Sn when undoped wires are desired (see Fig. 5).

2.4.3. Type C Catalysts

This is the group of catalyst metals that may form one or more silicide phases. Usually, the PDs of type C catalysts are rather complex, with several silicide phases and various eutectic points. Due to the presence of the silicide phases, the type C catalyst offer, in addition to growth via the VLS mechanism, the opportunity of VSS wire growth via the solid silicide particle. This can be understood by considering the growth of Si nanowires with the help of Ti.[15,102,103] Figure 4 shows the Si-rich half of the Ti–Si PD depicted. As indicated therein, Ti–Si possesses an eutectic point at 1330 °C neighboring the pure Si side of the PD, so that the corresponding liquidus line can be used for Si wire growth via the VLS mechanism. If growth temperatures below 1330 °C are applied, growth should proceed via the phase that, at this temperature, is neighboring the pure Si side, that is, $TiSi_2$. Considering growth at 1000 °C starting from a Ti particle, the Ti particle will, due to the Si-rich conditions, transform into a Ti_5Si_3 particle, which transforms into Ti_5Si_4, which transforms into TiSi, which finally transforms into $TiSi_2$. Only when this transformation process is completed, Si-wire growth can start. Si-nanowire growth via the VSS mechanism catalyzed by a $TiSi_2$ particle has first been observed by Kamins et al.,[102] who synthesized Si nanowires at 640–670 °C by means of CVD process. The main advantage of Ti lies in the favorable positioning of its impurity level (see Fig. 5) and in the fact that Ti or $TiSi_2$ is deemed compatible with CMOS technology. However, the crystallographic quality of Si nanowires grown via $TiSi_2$ catalyst particles seems to be poor compared to what can be obtained by using Au as catalyst.

Similarly to Ti, the use of Fe or Dy as catalyzing impurities in CVD processes at temperatures around 600 °C leads to the growth of Si nanowires with a high density of crystallographic defects.[89] This seems to be more a general effect of VSS growth via silicide particles than a property of a specific metal, as Morales and Lieber[7] demonstrated that nanowires of high crystalline quality can also be synthesized using Fe. They used a Nd-YAG laser to ablate material from a mixed Fe–Si target within a quartz furnace heated to very high temperatures. In this way, they obtained $\langle 111 \rangle$ oriented Si nanowires, presumably grown via the VLS mechanism.

The noble metals Pd and Pt are known to have similar physical and chemical properties. According to their PDs with Si, both noble metals require high temperatures for VLS growth; 892 °C in case of Pd, 979 °C in case of Pt. Applying such high temperatures, similar results as with Au as catalyst have been obtained.[5] This can best be seen in the works of Weyher[99] and Wagner and Ellis,[2] who both used $SiCl_4$ CVD processes to synthesize Pt-catalyzed Si wires via the VLS mechanism at temperatures around 1000 °C. Both obtained $\langle 111 \rangle$ oriented wires with hexagonal cross-sections and {211} side faces. A very interesting result has been reported by Bootsma and Gassen,[78] who claim that "Filamentary growth was also obtained with Ag, Cu, Ni, and Pd at substrate temperatures of about 800 °C". This is insomuch surprising as, according to their PDs, all of these metals require temperatures of more than 800 °C for VLS Si wire growth (see Fig. 5). In the case of Pd, the reported growth temperature is almost 100 K below the minimum temperature required for VLS growth. Of course, one always has to take into account the possibility that the catalyst particle is in a metastable undercooled state, so that albeit the low temperature, growth proceeds via the well known VLS mechanism. Growth via the VSS mechanism, employing a solid silicide particle provides another plausible explanation. According to the Pd–Si PD, one can expect that VSS growth at 824–892 °C is mediated by a PdSi silicide particle, whereas at temperatures below 824 °C VSS growth should be catalyzed by a Pd_2Si particle. Recently, circumstantial evidence for VSS Si nanowire growth via a Pd–silicide particle (presumably Pd_2Si) has been given by Hofmann et al.[13] They used in situ transmission electron microscopy (TEM) to study the growth of Si nanowires at temperatures around 892 °C, and found that Si-nanowire growth works via lateral ledge flow at the silicide–silicon interface. Concerning the possible silicides, the situation is less complex for Pt. According to the Pt–Si PD, growth

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim
WILEY InterScience DISCOVER SOMETHING GREAT

should proceed via a solid PtSi particle at temperatures below 979 °C. Consistently, Baron et al.[100] demonstrated VSS Si nanowires growth using PtSi catalyst particles at temperatures as low as 500 °C. Similar results have also been obtained by Garnett et al.[101]

Cu and Ni as well are very interesting catalyst materials from an electronics point of view: Cu, like Au, is a very efficient recombination center in Si, and is interesting because Cu is already used for interconnects in integrated circuits (ICs), so that Cu cannot be considered CMOS incompatible; Ni, because its impurity levels in Si (see Fig. 5) are not too close to the band-gap middle and because Ni–silicide electrical contacts are well-known standard contacts in IC technology. The minimum temperature required for VLS Si wire growth using Ni is 993 °C, about 200 K higher than that of Cu (802 °C), and at high temperatures both Cu and Ni are known to produce Si-wire growth results comparable to those obtained with Au.[2,28] The fact that excellent Si wires can be grown with Cu has recently been demonstrated by Kayes et al.[88] They managed to synthesize large arrays of perfectly aligned ⟨111⟩ oriented Si wires with both Au and Cu as catalyst in a $SiCl_4$ CVD process at temperatures of 850–1100 °C. But not only VLS growth, also VSS growth using Cu has been demonstrated. Yao and Fan[86] claim to have grown ⟨111⟩ Si nanowires at 500 °C via the VSS growth mode using a SiH_4 CVD process. In consistence with the Cu–Si PD, they found a Cu_3Si silicide particle at the tip of the nanowires. Unfortunately, the obtained Si nanowires show of a significant number of crystallographic defects. Similar results were obtained by Arbiol et al.[87]

To conclude, the type C catalysts work well but just in the VLS mode (at high temperatures). At temperatures below the eutectic, problems with the crystalline quality of the wires arise. The type B catalysts In and Ga work but only under harsh experimental conditions (high temperature or plasma assisted). Growth using Zn seems to be easier compared to In or Ga, but there is no real advantage of Zn compare to Au. Thus, for low-temperature CVD, everything boils down to the use of the three type A catalysts, Au, Al, and Ag.

3. Thermodynamics of VLS Wire Growth

3.1. Expansion of the Nanowire Base

The expansion of the nanowire base during the initial phase of growth provides a good example for the interplay between droplet and nanowire in the VLS growth mechanism. However, before coming to this, some brief remarks on the use of the terms surface stress, surface tension, and surface free energy, because this sometimes causes confusion. This confusion arises because, unlike in liquids, the surface free energy and the surface tension (or surface stress, respectively) of a solid are not necessarily equal. This has first been pointed out by Gibbs[110] and later discussed also by Shuttleworth.[111] The surface free energy is related to the work of creating new area, for example by splitting, whereas the surface stress is related to the work of increase in the surface area by elastic deformation.[112] This work for the increase in the surface area of a solid by elastic deformation can be characterized by a second rank tensor, the surface stress tensor. Considering isotropic surfaces, this tensor reduces to a scalar quantity often simply called surface stress. We will neglect this differentiation and bluntly refer to it as the surface tension of the solid.

Another concept that was also first brought up by Gibbs is that of a line tension. Gibbs pointed out[113] that, completely analogously to the concept of surface tension, a line tension τ should be assigned to dividing lines between different phases. In our case, this concerns the perimeter of the droplet–silicon interface, where vapor, liquid, and solid phases meet. Including the line tension would lead to an additional τ/r term in the equilibrium conditions, with r being the radius of the circular contact line. The value of the line tension is usually estimated to be in the range 1×10^{-11}–1×10^{-9} J m^{-1}.[114] So one can easily figure out that, compared to the surface tensions typically being on the order of 1 J m^{-2}, a line tension contribution can safely be neglected unless the radius r is on the order of a few nanometers; even then, it is unclear how significant the influence of the line tension really is. Therefore, a line tension contribution will be neglected in the following.

This subsection is dedicated to the description of an effect that is observed for Si wires grown epitaxially on Si substrate, namely that the wire diameter is enlarged in the region where the wire is connected to the substrate (see, for example, refs. [2,115–117] or Fig. 8). In effect, the body of the wires grown via the VLS mechanism exhibits a typical expansion. Without considering the special implications of the VLS growth mechanism, one might be tempted to assume that an overgrowth of Si could provide a sensible explanation. Two arguments, however, speak against this. The first, put forward by Givargizov,[118] is that the observed diameter expansion at the wire base does not depend—or at least only weakly—on the growth temperature applied. The second is that the shape of the expansion approximately scales with the diameter of the wire. Consequently, Givargizov concluded that the "conical expansion at the whisker root must not be mistaken with an expansion due to overgrowth"[118] and that "the transition is evidently related to a change of the contact angle configuration".[118]

The fact that there must be some change of the contact angle (defined here as the angle within, in the liquid) becomes apparent if the typical shapes of droplets on flat Si substrates are compared to those on top of Si wires. According to Ressel et al.,[119] Au–Si alloy droplets on flat Si substrates and at temperature between 400 and 650 °C show a contact angle of $\beta_0 = 43°$. In contrast, as can be seen, for example, in the work of Kodambaka et al.,[9] Au–Si droplets on top of wires are much more spherical, typically exhibiting contact angles of the order of 120°. Clearly, the droplet shape must undergo some transition in the initial phase of growth, and as schematically shown in Figure 7, this change in shape induces the observed expansion of the wire base. Several attempts have been made in the past to qualitatively simulate this expansion,[116,120–122] and here we will follow the work of Schmidt et al.[122] Please note that the model for the expansion of the nanowire diameter at its base cannot be applied to templated nanowire growth (see, for instance, refs. [24–26]) as the nanowire diameter is confined by the diameter of the template pore.

With the line tension omitted, the three quantities necessary to describe the contact-angle configuration of the droplet are σ_l, the surface tension of the liquid (the catalyst droplet), σ_s, the surface of the solid (the Si wire), and σ_{ls}, the surface tension of

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

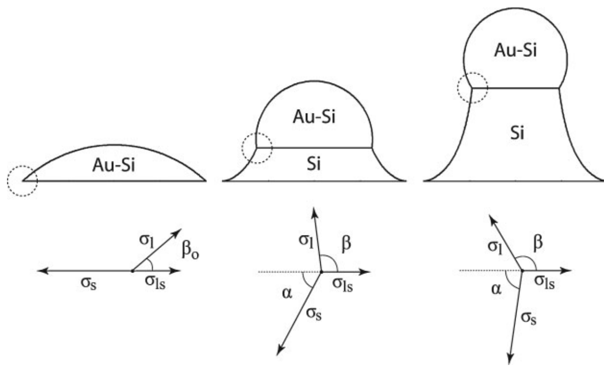

Figure 7. Schematic development of the droplet and wire shape in the initial phase of VLS wire growth. The shape corresponds to the calculated shape assuming $\sigma_s = 1.24$ J m^{-2}, $\sigma_s = 0.85$ J m^{-2}, and $\sigma_{ls} = 0.62$ J m^{-2}. Below, the corresponding equilibrium balance of surface forces (at the left edge of the droplet) is indicated. Note that the horizontal force components add up to zero.

the liquid–solid interface. For brevity, σ_{ls} is referred to as a surface tension instead of an interface tension, as would be more precise. If the wire-growth velocity is small compared to the reaction velocity of the droplet, the development of the droplet–wire system can be described in a quasi-static growth model. This means the shape of the droplet may undergo a transition, but the development corresponds to a sequence of equilibrium states. At equilibrium, the contact angle β of the droplet is related to the inclination angle α and the surface tension values σ_s, σ_l, and σ_{ls} by the Neumann triangle relation.[123,124]

$$\sigma_l \cos(\beta) = \sigma_s \cos(\alpha) - \sigma_{ls} \tag{1}$$

For $\alpha = 0$, Equation (1) reduces to Young's well-known equation. Equation (1) means nothing more than that, in equilibrium, the horizontal components of the surface forces have to cancel each other, such that there is no net force acting on the perimeter of the droplet. This is shown in Figure 7, where the balance of surface forces is displayed at three different stages of growth. With the shape of the droplet taken as the segment of a sphere, the radius r of the liquid–solid interface can be expressed as a function of the contact angle β (measured in the liquid) and the volume V of the droplet.

$$r = \left(\frac{3V}{\pi}\right)^{1/3} \frac{(1+\cos(\beta))^{1/2}}{(1-\cos(\beta))^{1/6}(2+\cos(\beta))^{1/3}} \tag{2}$$

The volume V of the catalyst droplet in turn is given by the initial conditions, that is, by the initial radius of the liquid–solid interface r_0 and the initial contact angle β_0; initial meaning here prior to growth, that is, at $\alpha = 0$.

$$V = \frac{\pi}{3}\left(\frac{r_0}{\sin(\beta_0)}\right)^3 (1-\cos(\beta_0))^2(2+\cos(\beta_0)), \tag{3}$$

Furthermore, the angle α, the inclination angle of the wire flanks, is trivially related to the slope of the wire via

$$\frac{\mathrm{d}h(r)}{\mathrm{d}r} = -\tan(\alpha), \tag{4}$$

with h being the height of the wire. The differential Equation (4) can be solved for h by simple integration. By combining Equation (1–4) and performing a numerical integration (easiest done using $\cos(\alpha)$ as integration variable), we can obtain the shape of the wire expansion for a certain configuration of surface tensions. Considering VLS Si-wire growth using Au as catalyst, the surface tension of the liquid droplet $\sigma_l = 0.85$ J m^{-2},[125] the surface tension of Si $\sigma_s = 1.24$ J m^{-2},[126] and the initial contact angle $\beta_0 = 43°$[119] can be used to calculate the liquid–solid interface tension, $\sigma_{ls} = 0.62$ J m^{-2}. The simulated shape of the wire expansion using these values is shown in Figure 7.

Figure 8 shows a TEM image of the expansion of the nanowire base. The white line corresponds to the calculated shape assuming $\sigma_s = 1.24$ J m^{-2}, $\sigma_l = 0.85$ J m^{-2}, and $\sigma_{ls} = 0.62$ J m^{-2}. One can see that there is good, though not perfect, agreement between experiment and theory. Notably, however, no fitting parameters whatsoever were used. The fact that the curve on the rhs of Figure 8 fits better than the one on the lhs is probably due the fact that the nanowire nucleated at a surface step.

To conclude, by considering the equilibrium balance of surface and the corresponding droplet shape, a model for the expansion at the wire was derived, which gives a reasonable qualitative description for the experimentally observed phenomenon.

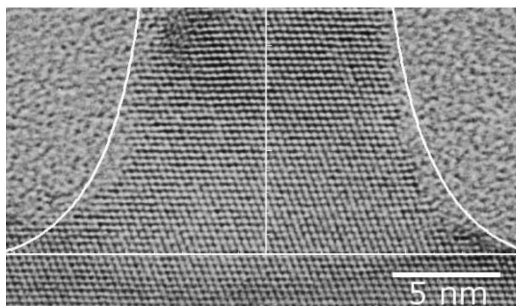

Figure 8. Transmission electron microscopy image of an epitaxially grown Si nanowire. The white line corresponds to the calculated shape assuming $\sigma_s = 1.24$ J m^{-2}, $\sigma_s = 0.85$ J m^{-2}, and $\sigma_{ls} = 0.62$ J m^{-2}.

3.2. Nebol'sin Stability Criterion

In the discussion of the different catalyst materials, it became clear that the growth of Si wires with the type B metals turns out to be more difficult than one might think in the first place. This could, for one thing, be a direct cause of the low Si solubility at the respective growth temperature. Surface tension could provide an alternative explanation. As we will see, following the work of Nebol'sin et al.[8] a certain minimum value for σ_l, the surface tension of the droplet, is required to allow for stable VLS wire growth.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

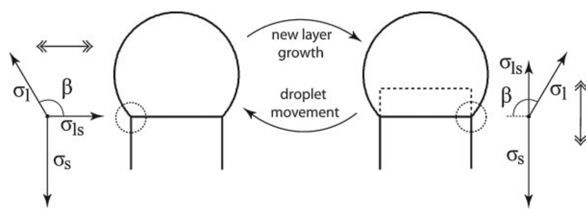

Figure 9. Si wire growth as a repetition of two consecutive growth steps shown on the lhs and rhs. On the lhs the force balance in horizontal direction has to be taken into account, on the rhs, the force balance of the vertical force components needs to be considered.

Let us consider the situation shown on the lhs of Figure 9, and let us assume, as indicated by the horizontal arrow, that the droplet can freely adjust its perimeter according to the balance of surface forces acting on the droplet. As discussed already, this implies that there is no horizontal net force acting on the droplet, or equivalently, that the horizontal components of the surface forces cancel out (see the lhs of Fig. 9). This is the case if

$$\sigma_l \cos(\beta) = -\sigma_{ls} \quad (5)$$

Equation (5) is equivalent to the equilibrium condition of Equation (1), with $\alpha = 90^\circ$.

The stability criterion can be derived by making a simple gedankenexperiment, depicted in Figure 9. Let us assume that Si-wire growth proceeds by the continuous repetition of two alternating growth steps—step one, the nucleation and growth of a new layer of Si at the droplet Si interface, and step two, the upward movement of the droplet to the edge of the newly grown layer. After step one, that is, the growth of the new layer, indicated in Figure 9 by a dashed line, the situation corresponds to what is schematically depicted on the rhs of Figure 9. As shown therein, the growth of the new layer causes the droplet to wet the side surface of the wire. The droplet has only one degree of freedom, namely the vertical position of its triple phase line. Consequently, the vertical surface force components have to be considered. In order for the droplet to recover its starting position, it is necessary for the droplet to move its triple phase line upward by an amount equal to the thickness of the newly grown layer, that is, the droplet has to dewet the side-surface portion of the new layer. This is only possible if there exists a net force component pointing upwards, which according to the force balance scheme shown on the rhs of Figure 9 corresponds to the following equality.

$$\sigma_l \sin(\beta) + \sigma_{ls} > \sigma_s \quad (6)$$

Combining Equations (5) and (6) the following condition is obtained

$$\sin(\beta) - \cos\beta > \sigma_s/\sigma_l \quad (7)$$

Since $\sin(\beta) - \cos(\beta)$ can maximally reach a value of $\sqrt{2}$ (at $\beta = 135^\circ$), condition (7) can only be fulfilled if

$$\sigma_l > \sigma_s \big/ \sqrt{2} \quad (8)$$

This is the Nebol'sin stability criterion. Adopting the value also used by Nebol'sin et al.[8] of $\sigma_s = 1.2\ \mathrm{J\ m^{-2}}$ for Si, we obtain a lower threshold for σ_l of about 0.85 J m^{-2}. If the surface tension σ_l of the liquid droplet is smaller than about 0.85 J m^{-2}, the droplet is not capable of dewetting the side surfaces of the wire. Droplets with too-small surface tensions do not sit on top of cylindrical Si wires.

The criterion (8) proves to be particularly useful if applied to the different VLS catalyst materials. Nebol'sin et al.[8] reported on both the surface tension values of various catalysts and on the corresponding stability of wire growth. Again, the catalyst classification introduced in Figure 6 turns out to be helpful. Nebol'sin et al.[8] report high surface-tension values of >1.3 J m^{-2} for the type B metals Cu, Pt, and Ni, and, as expected, the reported growth stability is correspondingly high. The surface-tension values of the three type A metals Ag, Au, and Al, are already considerably lower, having values of about 0.9 J m^{-2} (Au and Ag), and 0.8 J m^{-2} Al.[8] Since this is at the limit of $\sigma_l = 0.85$ J m^{-2}, we expect a change of the growth characteristics; and indeed, according to Nebol'sin et al.,[8] the growth stability changes, being high for Au but low for Al. The type C metals, Bi, Sb, Pb, Sn, Zn, In, and Ga, do have even lower surface tension values, ranging from 0.6 to 0.8 J m^{-2} for Sn, Ga, and Zn,[8,127–129] to values of around 0.4 J m^{-2} for Bi, Sb, Pb.[8,128,130,131] The overall tendency that wire growth becomes more and more difficult with smaller surface-tension values of the liquid still holds. According to Nebol'sin et al.,[8] only a low growth stability can be achieved with Zn (0.8 J m^{-2}[129]), and no wires at all can be grown with Bi, Sb, and Pb (0.4 J m^{-2}). An exception to the rule seems to be In, for which wire growth has been reported by several authors,[8,16,85,93,95] despite its low surface tension of about 0.5 J m^{-2}.[8,132]

3.3. Growth Velocity and Gibbs–Thomson Effect

The chemical potential μ is the energetic "price" per atom if another atom of the same species is added to the system. For small systems, that is, systems having high surface-to-volume ratios such that the influence of the surfaces on the thermodynamics cannot be neglected, it is clear that increasing the number of atoms N implies an increase in the surface area, and that one has to pay the energetic price for that surface increase as well. Considering a spherical droplet of radius R and volume $4\pi/3R^3 - N\Omega$, with Ω being the volume per atom (assumed to be constant here), the Gibbs-free energy G can be written as $G = \mu_\infty N + 4\pi R^2\sigma$, with σ being the surface free energy and μ_∞ being the bulk (infinite radius) chemical potential. Using $\partial R/\partial N = \Omega/(4\pi R^2)$, one can easily find that the chemical potential $\mu = \partial G/\partial N$ becomes $\mu = \mu_\infty + 2\Omega\sigma/R$. This is the Gibbs–Thomson effect.

The treatment is very similar for a cylindrical wire; yet, one has to be careful with which values are constant and which are not. The Gibbs free energy of a wire of length L, radius r, and surface free energy σ can be expressed as $G = \mu_\infty N + 2\pi r^2\sigma + 2\pi rL\sigma$. Assuming that the nanowire only grows in length, assuming the radius to be constant, and using $\partial L/\partial N = \Omega/(\pi r^2)$, the chemical potential $\mu = (\partial G/\partial N)_r$ becomes[118]

$$\mu = \mu_\infty + \frac{2\Omega\sigma}{r} \quad (9)$$

which is an expression very similar to that for a sphere. Note that the factor of 2 in the numerator only occurred because the radius

WILEY InterScience® DISCOVER SOMETHING GREAT

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

was taken to be constant. If an infinitely long wire that expands in circumference but not in length is considered, then an equation similar to (9) is obtained, yet without the factor of 2; This is emphasized here only because there seems to be some confusion in the literature whether or not there should be a factor of 2 in the Gibbs–Thomson formula for cylindrical nanowires.

The Gibbs–Thomson effect of course affects the nanowire growth velocity. It causes the growth velocity to become radius dependent, an effect observed by several researchers.[6,10,99,133–136] In some sense, this radius dependence of the growth velocity depends on which is the rate determining step of CVD wire growth via the VLS mechanism. Following Givargizov,[6] one can subdivide the growth process into three main substeps. First, the gaseous Si precursor is cracked at the surface of the catalyst droplet, Si is released, and it gets incorporated into the droplet. This step will be called incorporation step, and it proceeds at a rate [atoms s^{-1}] called the incorporation rate. Following incorporation, Si dissolved in the droplet diffuses from the droplet surface to the nanowire/droplet interface. This is the second step, the diffusion step. In the last step of the process, Si crystallizes at the liquid–solid interface and forms the Si nanowire. This will be called the crystallization step, proceeding at a rate [atoms s^{-1}] called the crystallization rate.

The diffusion step can presumably be neglected. Diffusion through a microscopic or even nanoscopic droplet is simply too fast as to seriously affect the growth velocity.[118] There was some discussion in the past as to which is the true rate-determining step, the incorporation or crystallization step. Bootsma and Gassen[78] argued that the growth velocity evidently depends on the precursor pressure, and concluded that incorporation is therefore the rate-determining step. This was opposed by Givargizov,[118] whose argument in favor of the crystallization step as the rate determining step is mainly based on the observation that the growth velocity depends on the crystallographic growth direction of the wires. However, this apparent dilemma can trivially be solved if the assumption of a single rate-determining step is discarded, and if it is instead assumed that the interplay between both steps determines the rate of growth.

The decisive parameter for the growth velocity is the Si supersaturation, which is defined as the difference between the Si chemical potential in the droplet and in the nanowire. Without a sufficient supersaturation, there will be no crystallization of Si at the liquid–solid interface, and therefore no growth. Hence, the crystallization rate should be a function of the supersaturation, and one can assume that the crystallization rate does increase with increasing supersaturation. Let us assume for now that the incorporation rate also depends on the supersaturation. The case where it does not can then still be derived as limit of the general expressions. Since an increase in the supersaturation reduces the chemical-potential difference between Si in the vapor and Si in the droplet, one could expect that the incorporation rate decreases with increasing supersaturation.

In any case, it should be clear that under steady-state growth conditions, the incorporation rate has to equal the crystallization rate. This steady-state condition demanding equal rates couples the incorporation and crystallization steps, and as a result of that the supersaturation under steady-state conditions will adjust at a level where both rates are equal. However, the level at which the steady state supersaturation $\Delta\mu$ will finally settle depends on the dependencies of the both incorporation and crystallization rates with respect to the supersaturation. To conclude, one can expect the growth velocity to generally depend on the interplay between the incorporation and the crystallization processes. On the one hand, this solves the dilemma concerning the discussion on the rate determining step, but on the other hand it renders the process more complicated.

Transforming the rates [atoms s^{-1}] into velocities [m s^{-1}] by multiplying them with $\Omega/(\pi r^2)$, we obtain the incorporation and crystallization velocities. At steady state, the incorporation and crystallization velocities have to be equal, which corresponds to a crossing of the two velocity curves in a velocity versus supersaturation space. The position of this crossing point then defines the steady-state growth velocity v and the steady-state supersaturation $\Delta\mu$. We can then define α, the derivative of the incorporation velocity with respect to the supersaturation at $\Delta\mu$, and ω, the derivative of the crystallization velocity with respect to the supersaturation at $\Delta\mu$. Using these derivates and performing a Taylor expansion to first order around the crossing point, one can obtain a general expression for the steady-state supersaturation

$$\Delta\mu = \Delta\mu_\infty + \frac{\alpha_1}{\omega_1 - \alpha_1}\frac{2\Omega\sigma}{r}, \quad (10)$$

and the steady-state growth velocity

$$v = v_\infty + \frac{\omega_1\alpha_1}{\omega_1 - \alpha_1}\frac{2\Omega\sigma}{r}, \quad (11)$$

where $\Delta\mu_\infty$ and v_∞ are the steady state supersaturation and the steady state growth velocity at infinite radius, that is, for macroscopic wires. Ω and σ are the volume per atom and the surface free energy of silicon, respectively. For a more detailed treatment, see Schmidt et al.[137] In this linear approximation, both $\Delta\mu$ and v are expected to show a $1/r$ dependence, but with a prefactor determined by the slopes of the incorporation and crystallization velocities. Keeping in mind that, as discussed above, one usually expects α to be negative and ω to be positive, both prefactors in (10) and (11) become negative. Consequently, $\Delta\mu$ and v are expected to decrease with decreasing radius. This $1/r$ behavior with negative prefactor as implied by (11) is indeed a reasonable first-order assumption, as shown in Figure 10 using data from Schmid et al.[136]

Notably, however, the first-order expression (11) does not suffice, in some cases, to provide a satisfyingly accurate description of the radius dependence of the growth velocity (see refs. [6,10,99]). Givargizov,[6] for example, fitted his growth velocity data with a function $v = (c_1 + c_2/r)^2$ with constants c_1 and c_2; in this case, an additional $1/r^2$ term was necessary, which can be obtained by going beyond the linear approximation.

One can now use the general expressions (10) and (11) to derive the special cases where one of the steps becomes rate determining. In the limit ($\alpha \rightarrow \infty$), the case where the crystallization is rate determining, one obtains

$$\Delta\mu = \mu_\infty - \frac{2\Omega\sigma}{r} \quad (12)$$

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

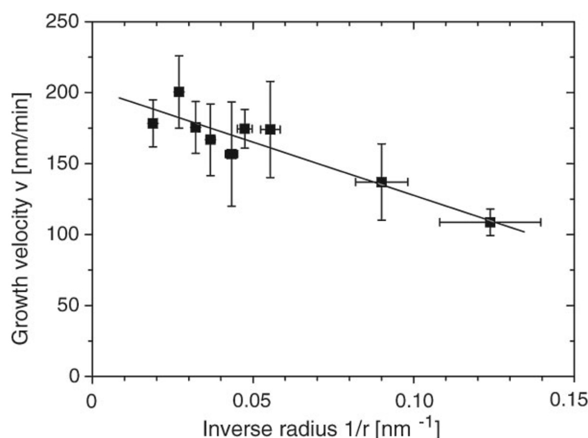

Figure 10. Nanowire growth velocity as a function of the inverse nanowire radius; data taken from Schmid et al.[136]

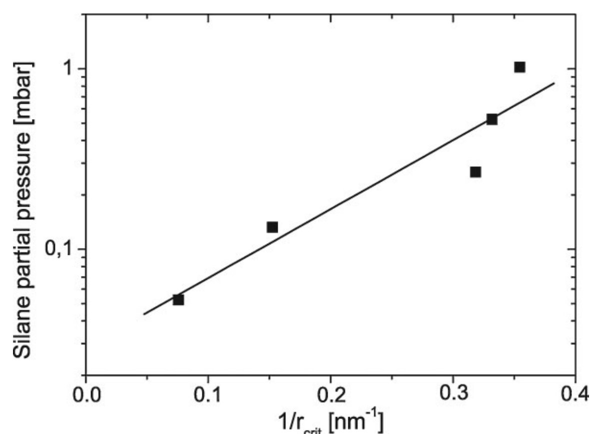

Figure 11. Silane partial pressure versus the corresponding inverse critical radius r_{crit}. Data taken from Dhalluin et al.[140] The slope of the linear fit is about 8.8 nm

This is equivalent to the result derived by Givargizov.[6] The special case mentioned before, where the incorporation velocity does not depend on the supersaturation, can be obtained by taking the limit ($\alpha \rightarrow 0$), in which case the radius dependence vanishes; consistently to what has been reported by Kodambaka et al.[9]

Another effect of the above-described radius dependence is that there should exist a critical minimum radius for which the growth velocity falls to zero. This should occur when $\Delta\mu$ becomes zero, or at least so small as to prevent further Si crystallization. The idea of a critical radius was first formulated by Wagner and Ellis,[2] and a thorough treatment on this subject has been published by Tan et al.[138,139] With $\Delta\mu_\infty$ in (10) being a function of pressure p and temperature, the critical radius also becomes temperature and pressure dependent. Assuming that (12) approximately holds (assuming that the crystallization determines the growth rate), approximating μ_∞ by $\mu_\infty = kT\ln(p/p_o)$, with p_o being some equilibrium pressure, and setting (12) to zero, one arrives at the following expression for the critical radius

$$r_{crit} = \frac{2\Omega\sigma}{kT\ln(p/p_o)} \tag{13}$$

Recently, a very interesting experimental study on this subject by Dhalluin et al.[140] was published. They employed the fact that the side faces of Si nanowires tend to be decorated with tiny Au islands.[20,41,141] They increased the silane pressure beyond the point where nanowires started to grow via these nanometer-sized Au islands, and then determined the radius of the smallest nanowires that still grew under the applied pressure. As expected, Dhalluin et al.[140] found that indeed higher pressures are necessary to grow smaller nanowires, and they presented a sophisticated model to explain this observation. Their data, however, can also be reasonably well explained by simply taking the Gibbs–Thomson effect into account. Solving (13) for $\ln(p)$ gives $\ln(p) = \ln(p_o) + (1/r_{crit})2\Omega\sigma/kT$. Thus, plotting the logarithm of the pressure as a function of the corresponding inverse critical radius r_{crit} should give a straight line with slope equal to $2\,\Omega\sigma/kT$. This is shown in Figure 11, with the pressure data of Dhalluin et al.[140] displayed on a logarithmic scale as a function of the inverse critical radius. One can see that their data points roughly lie on a straight line, the slope of which is ~8.8 nm. Using this value together with $\Omega = 0.02$ nm^3,[142] the Boltzmann constant, and the temperature of 773 K, reported by the authors,[140] one can deduce a surface free energy σ of about 2.3 J m^{-2}. This value is in surprisingly good agreement with the surface free energy of a Si (100) surface, reported to be around 2 J m^{-2}.[126,143]

4. Electronic Properties of Silicon Nanowires

Considering bulk Si, it is easy to determine the dopant concentration. By measuring the resistivity (by four-probe measurements) and using existing calibration curves (see, for example, ref. [142]) one can relate the resistivity to the impurity concentration. For Si nanowires, however, using this bulk Si calibration curves may in many cases be misleading. This has been shown, for example, by Wang et al.,[19] who determined the resistivity of phosphorous-doped Si nanowires from four-probe measurements and the corresponding dopant concentration, N_D^0, using secondary-ion mass spectroscopy (SIMS). Comparing these results to the resistivity versus P concentration curves of bulk Si, one can figure out that the resistivity of the nanowires is about one to two orders of magnitude larger than the resistivity of bulk Si of the same dopant concentration. Or, from another angle, if the authors had measured the resistivity and used the bulk Si calibration curve for P to deduce the dopant concentration, they would have underestimated the P concentration by about a factor 10–100. One can see that by applying the bulk-Si resistivity versus dopant concentration curves to Si nanowires, one is walking on thin ice, and there is a good chance that the results are significantly wrong.

Even at diameters $\gtrsim$10 nm, a size where quantum-confinement effects can to a good approximation still be neglected, nanowires may behave differently from bulk material. According to Ohm's law, the conductivity of p-type bulk Si, for example, is proportional to the product of the hole density, p, and the corresponding mobility μ_p. Concerning the charge-carrier density, one is used to

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

equating the hole concentration p with the concentration of acceptor atoms, N_A^0 (subscript A for acceptor). Yet, one has to be careful, because setting N_A^0 equal to p implies that three separate approximations hold. First, that the total acceptor concentration N_A^0 equals the concentration of electrically active acceptors, N_A. Second, that the electrically active acceptors are fully ionized, so that $N_A = N_A^-$, with N_A^- being the concentration of ionized acceptors. And third, that $N_A^- = p$, that is, the hole concentration is fully determined by the acceptor density. For n-type Si, we can analogously write $N_D^0 = N_D$, $N_D = N_D^+$, and $N_D^+ = n$, with N_D^0 being the total concentration of donors. In the following three subsections, the limits of validity of these three approximations is reviewed. The subsection following thereafter is dedicated to mobilities in Si nanowires.

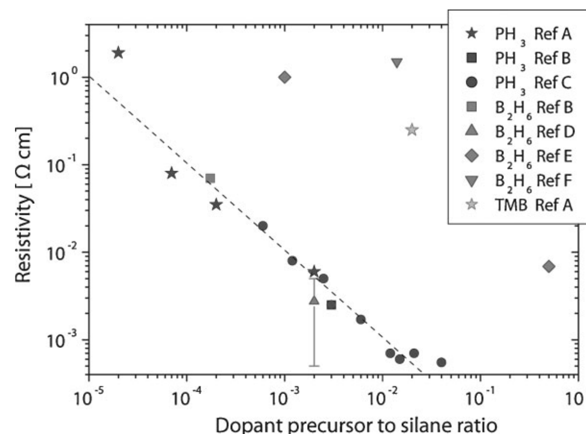

Figure 12. Si nanowire resistivity versus dopant precursor to silane ratio. Data taken from Ref A [19], Ref B [136], Ref C [190], Ref D [191], Ref E [154], Ref F [153]. The dashed line has slope −1.

4.1. Doping

The functionality of semiconductor devices crucially depends on the possibility of variably adjusting their electronic properties by the addition of dopants. These are shallow-level impurities, such as B, P, As, Ga, Al, or Sb (see Fig. 5), whose main purpose is to tune the position of the Fermi level within the Si band-gap, such that type and concentration of the majority charge carriers can be defined by the dopant concentration. One additional complication that has to be considered here is that the dopants need to be substitutionally incorporated within the silicon lattice in order to become electrically active.[144] Thus, one has to be precise about what is meant by dopant concentration. On the one hand you have the total donor (acceptor) concentration N_D^0 (N_A^0). This is the value you would obtain by counting the number of dopant atoms within a certain volume, for example, by analyzing the composition of the nanowire using SIMS. Whether these dopants are electrically active or not depends on their local environment. Usually, dopants need to be substitutionally incorporated within the Si lattice. Under certain conditions, the density of electrically active donors (acceptors), N_D (N_A) might therefore differ from their total concentration, N_D^0 (N_A^0). One could imagine that the dopant atoms, though being present, are not properly substitutionally incorporated, a scenario that can occur after dopant implantation and which is one of the reasons why additional thermal treatment is required after implantation. Another possible cause could be that dopant atoms are located at the nanowire surface, rendering them electronically inactive. In this way, they would be counted by SIMS measurements but would not affect the electronic properties. At least for very thin Si nanowires, calculations showed that there indeed exists a certain tendency of B or P atoms to diffuse to the surface.[145]

Naturally, there are different ways to dope Si nanowires. One way would be the use of a catalyst metal that by itself may act as a dopant for Si. This mainly concerns the growth of Si nanowires using In,[16,95] Ga,[15,84,94] or Al.[11,16,81,84] Despite good reasons to believe that the resulting wires are indeed highly p-doped, a direct evidence for the effectiveness of such an approach still seems to be missing. Alternatively, one could add a small amount of the chosen dopant to the Au catalyst droplet in the hope that the dopant will be released and incorporated during wire growth. The feasibility of such an approach has been demonstrated;[146] however, the method seems to be ineffective.

An approach that offers much better controllability concerning dopant type and density is to supply the dopant during growth. This can be done by co-evaporation of Si and dopant for MBE nanowire growth,[42] coablation of the Si and dopant for nanowire growth by laser ablation,[147–149] or cosupply of Si and dopant in form of gaseous precursors for CVD nanowire growth.[150,151] Since the overall focus of this article is on CVD Si-wire growth, let us now take a closer look on the in situ doping of CVD grown wires. Figure 12 shows a collection of resistivity versus dopant precursor to silane (SiH_4) mixing ratio data for different dopant precursors such as phosphine (PH_3), diborane B_2H_6, and trimethylborane (TMB), $B(CH_3)_3$.

The PH_3 data presented in Figure 12 show in a surprisingly coherent manner that the resistivity can be varied over orders of magnitude by changing the PH_3/silane ratio; and, most importantly, that the resistivity is approximately inversely proportional to the PH_3:SiH_4 ratio, so that doubling the PH_3 supply really halves the resistivity. This direct proportionality is indicated by the dashed line of slope −1. Furthermore, it has been reported[136] that PH_3 does not induce tapering of the nanowires by unwanted Si deposition on the side faces, and that the nanowire growth rate is almost unaffected. PH_3 therefore seems to be the precursor of choice for in situ n-type doping of Si wires. The only complication using PH_3 arises when PH_3:SiH_4 ratios greater 2×10^{-2} are applied, because in this case, nanowire nucleation seems to be inhibited[136]—similarly to what has previously been reported for the use of arsine[136] as n-type dopant. The addition of arsine is known to affect the growth of Si wires[6,152] presumably by changing the surface tension balance.

The resistivity data concerning the use of diborane as a p-type dopant precursor are far less consistent then the PH_3 data. One source of this inconsistency could be that the addition of diborane is known to trigger the growth of an amorphous Si shell.[153] With amorphous Si possessing a higher resistivity than crystalline Si, the presence of an amorphous shell could offer an explanation for the large resistivity reported by Lew et al.[153] and Cui et al.[154] One possible strategy to suppress the unwanted, diborane-induced deposition of Si on the wire surface could be to increase the hydrogen pressure, for it is known that hydrogen can

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim
WILEY InterScience DISCOVER SOMETHING GREAT

reduce the Si deposition rate[155,156] if silane is used as precursor. Another possibility to achieve p-type boron doping and to avoid an unwanted side deposition is to use TMB instead of diborane. Lew et al.[153] reported that the growth of Si nanowires without amorphous shell is possible if TMB is used. However, SIMS measurements performed on these wires indicated that the *B* incorporation efficiency is about two orders of magnitude smaller,[19] so that correspondingly higher TMB pressures need to be applied. In view of the lower efficiency of TMB, it is not surprising that the resistivity of these nanowires (see Fig. 12) is rather high.

As mentioned already, Wang et al.[19] not only measured the resistivity of the PH_3-doped nanowires, but also determined the donor concentration N_D^0 by performing SIMS measurements on these nanowires. Comparing these data with what is known from bulk Si, it becomes apparent that considering a specific dopant concentration, the resistivity of the nanowires is one to two orders of magnitude larger than the corresponding resistivity for bulk Si. One possible explanation is that a certain percentage of the donor atoms are not electrically active, or that surface states reduced the charge-carrier concentration. Another explanation is that the active dopant atoms are not fully ionized, a cause that is investigated in more detail in the following subsection.

4.2. Ionization Energy

Considering bulk Si, one is somehow used to the assumption that the dopant atoms are fully ionized, that is, to assume that the concentration of ionized donors N_D^+, for example, approximately equals the concentration of electrically active donors N_D. This is usually a fair approximation for bulk Si at room temperature doped with the standard dopants with ionization energies of about 50 meV. For Si nanowires, however, things might be different since the ionization energy, the energy difference between the donor (acceptor) level and the conduction (valence) band, depends on the electrostatics of the surrounding material. The reason why only so little energy is needed to ionize those impurities is due to the fact that the electrostatic potential of the ionized impurity is shielded by charge carriers in the Si. Hence, it is intuitively understandable that when the volume of Si surrounding the dopant atom is reduced, the shielding of the electrostatic potential is also reduced, in turn causing an increase in the ionization energy. Applied to Si nanowires, this means the ionization should be radius dependent, and should increase for decreasing nanowire radius. Furthermore, one can expect the effect to be more pronounced if the nanowire is surrounded by a medium of low dielectric constant.

Diarra et al.[157] investigated this effect, the increase in ionization energy of dopants in semiconducting nanowires due to the dielectric confinement, in detail. They report that the radius-dependent ionization energy $E_I(r)$ of a dopant can be expressed as

$$E_I(r) = E_I^0 + \frac{2}{R\varepsilon_s}\frac{\varepsilon_s - \varepsilon_{out}}{\varepsilon_s - \varepsilon_{out}} F\left(\frac{\varepsilon_s}{\varepsilon_{out}}\right) \quad (14)$$

with E_I^0 being the ionization energy of the dopant in bulk Si. ε_s and ε_{out} are the relative permittivity of the semiconductor

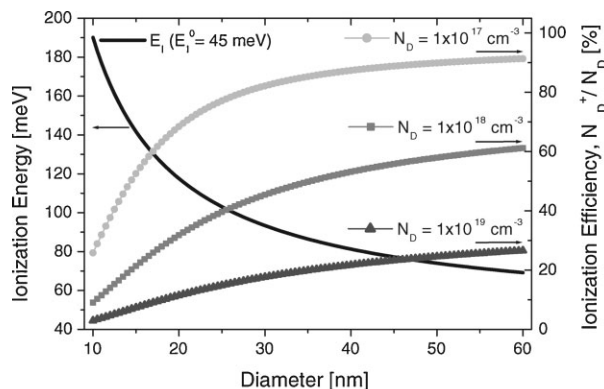

Figure 13. Ionization energy (scale on the lhs scale) and ionization efficiency (scale on the rhs) of *P* impurities ($E_I^0 = 45$ meV[157] in Si nanowires as a function of the nanowire diameter, after Diarra et al.[157] The ionization efficiency is given for various donor concentrations N_D and a temperature of 300 K.

nanowire and the medium surrounding the nanowire, respectively. According to Niquet et al.,[158] the function $F(x)$ can be approximated as

$$F(x) = \frac{200.674 + 175.739x + 17.395x^2 + 0.0949x^3}{219.091 + 50.841x + x^2} [\text{eV nm}] \quad (15)$$

Considering the ionization energy of a Si nanowire ($\varepsilon_s = 11.7$) in vacuum ($\varepsilon_{out} = 1$), we obtain $E_I(R) = E_I^0 + (1/r)725.5$ meV nm. The expressions by Diarra et al.[157] are only valid when additional quantum effects can be neglected, that is, for Si nanowires with diameters greater than ≈10 nm. The ionization energy of an impurity *P* in Si nanowires as a function of the nanowire diameter is shown in Figure 13. One can see that the ionization energy strongly increases with decreasing diameter, and that even at relatively large diameters of 30 nm, the ionization energy is still increased by about a factor of two.

Of course, a change in the ionization energy is accompanied by a change in the ionization efficiency, defined as the density of ionized dopants divided by the total density of dopants. In case of one dopant type being dominant, such that the contribution of the minority charge carriers to the charge balance can be omitted, the concentration of ionized donors N_D^+ or acceptors N_A^- is approximately given by[142,159]

$$N_D^+ = \frac{N_c}{4} e^{-E_I/kT}\left(-1 + \sqrt{1 + 8\frac{N_D}{N_C} e^{E_I/kT}}\right), \quad (16)$$

$$N_A^- = \frac{N_v}{8} e^{-E_I/kT}\left(-1 + \sqrt{1 + 16\frac{N_A}{N_V} e^{E_I/kT}}\right) \quad (17)$$

In Figure 13 the ionization efficiency of impurities *P* in Si nanowires is shown for three different donor concentrations N_D. One can see, that especially for thin Si nanowires with diameters

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

of 15 nm or less, the effect of the dielectric confinement on the ionization efficiency is quite pronounced. For Si nanowires with such small dimensions, the reduction of the ionization efficiency can be expected to have a non-negligible influence on the electric characteristics of the nanowires.[160] Consequently, the dielectric-confinement effect and its implications have to be taken into account.

4.3. Surface States and Charge Carriers

The singular property that renders Si such an advantageous material for electronics is that it possesses a chemically stable oxide, SiO_2, which can be produced in a way in which the Si surface is well passivated. A good oxide with a low level of charge stored in the oxide or at the Si/oxide interface is of utmost importance for Si-based electronics devices, such as field-effect transistors (FETs). The quality of the oxide and Si/oxide interface is, of course, not only important for traditional top-down Si devices but also for Si nanowires. In particular, for small diameters, that is, large surface-to-volume ratios, one can expect that the surface properties may significantly influence the electrical characteristics. The focus of this section will be to estimate the influence of the surface and the extent to which it changes the electrical properties of a nanowire.

Following the nomenclature of Deal,[161] one commonly distinguishes between four different categories of charges that may occur in or at the Si/SiO_2 interface. The first two categories correspond to charges that are located deep inside the oxide; this can be either oxide-trapped charges (density Q_{ot}) or the mobile ionic charges (density Q_m). Considering the charges at or in close vicinity of the Si/SiO_2 interface, one differentiates between the fixed oxide charges (density Q_f) and, most importantly, the interface trap charges (density Q_{it}). The main difference between the fixed oxide charges and the interface trap charges is that the fixed oxide charges, as the name implies, are fixed, and do not interact with the underlying Si in the sense that Q_f does not depend on the position of the Fermi level in Si. Therefore, the main effect of Q_{ot}, Q_m, and Q_f is a change in the electrostatics. Considering the characteristics of nanowire FETs, the effect of Q_{ot}, Q_m, and Q_f is to act as a fixed gate bias, that is, to simply shift the threshold voltage.

More interesting, and presumably also more important for the electrical properties, are the interface trap charges (density Q_{it}), because their density does depend on the position of the Fermi level in the Si, and they can exchange charges with Si. In fact, the interface trap-charge density Q_{it} is formed when states at the Si/SiO_2 interface trap or release single charge carriers. Since the density of these trap levels varies within the Si band-gap, they are characterized by an interface trap-level density D_{it} [$eV^{-1}\,cm^{-2}$]. As a function of energy, D_{it} of the Si/SiO_2 interface is U-shaped, with the minimum is located at the band-gap middle.[142,162] It was found that the presence of such interface trap states can be related to the presence of the so-called P_b resonance centers, observed in electron-spin-resonance experiments,[163–165] and it could be shown that these P_b centers are indeed the main source for interface trap states.[166–172] Concerning their physical nature, it was found that the P_b centers correspond to trivalent Si atoms bonded to just three other Si atoms.[167,173] Thus, loosely speaking, the interface trap states are nothing more than dangling bonds at the Si surface. Thinking of the interface states as dangling Si bonds, it is reasonable that the interface states are amphoteric, that is, they can act as donors and acceptors. The states below the band-gap middle are donor-like states (they are either neutral or positively charged), whereas the states above the band-gap middle are acceptor-like states (they are either neutral or negatively charged). Whether these states are charged depends on the position of the Fermi level at the surface. Considering n-type Si wires with their Fermi level located in the upper half of the band-gap, all interface trap states between the Fermi level and the band-gap middle will trap one electron and become negatively charged. The electrons for this maneuver have to be taken from the underlying Si, causing the Si to be depleted down to a certain depth. Schmidt et al.[174] investigated such a scenario in detail, adopting the full depletion approximation and taking the dopants to be fully ionized. In view of the discussion in the previous subsection on the increase in ionization energy, assuming the dopants to be fully ionized seems to oversimplify the complexity of the problem. However, the model of Schmidt et al.[174] can be easily extended to also cover the ionization effects, if it is assumed that ionization itself is not directly affected by the presence of interface states.

Consider an n-type Si nanowire of radius r with a density of ionized donors N_D^+, according to (16). In the absence of interface traps, the position of the Fermi level, ψ_o [eV], with respect to the band-gap middle would be

$$\psi_o = kT \ln\left[\frac{N_D^+ + \sqrt{(N_D^+)^2 + 4N_cN_v e^{-E_g/kT}}}{2N_c e^{-E_g/kT}}\right], \tag{18}$$

with N_c and N_v are the density of states in the conduction and valence band, respectively, and E_g the band-gap width. Introducing the parameter $\chi = q^2 N_D^+ r^2/(4\varepsilon_s\varepsilon_o)$, with ε_o being the vacuum permittivity and q the elementary charge, the radius r_d up to which the nanowire is depleted is given by

$$r_d = r\sqrt{1 - \left(\frac{2D_{it}\psi_o}{rN_D^+ + 2\chi D_{it}}\right)} \tag{19}$$

Here, of course, the interface trap-level density D_{it}, the source for the depletion, is included. The nanowire is said to be partially depleted when $0 < r_d < r$, and fully depleted when $r_d = 0$. For given values of D_{it} and N_D^+, full depletion occurs when the nanowire radius is smaller than a certain critical radius

$$r_{crit} = \frac{\varepsilon_s\varepsilon_o}{q^2 D_{it}}\left(-1 + \sqrt{\frac{4q^2 D_{it}^2\psi_o}{N_D^+\varepsilon_s\varepsilon_o}}\right) \tag{20}$$

In a good approximation, $r_{crit} \approx 2D_{it}\psi_o/N_D^+$. Solving the Poisson equation, one can calculate ψ_s [eV], the Fermi level (with

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

respect to the band-gap middle), at the nanowire surface

$$\psi_{\mathrm{s}} = \psi_{\mathrm{o}} - \chi \frac{\left(r^2 - r_{\mathrm{d}}^2\right)}{r^2} \tag{21}$$

The electron concentration averaged over the cross-section in case of a partially depleted nanowire is then given by

$$\overline{n}_{\mathrm{pd}} = N_{\mathrm{c}} e^{\left(\psi_{\mathrm{o}} - E_{\mathrm{g}}/2\right)/kT} \left(\frac{r_{\mathrm{d}}^2}{r^2} + \frac{kT}{\chi} \left(1 - e^{\frac{\chi\left(r_{\mathrm{d}}^2 - r^2\right)}{kTr^2}} \right) \right) \tag{22}$$

For a fully depleted nanowire, we obtain the following average electron concentration.

$$\overline{n}_{\mathrm{fd}} = N_{\mathrm{c}} e^{\left(\psi_{\mathrm{s}} - E_{\mathrm{g}}/2\right)/kT} \frac{kT}{\chi} \left(e^{\chi/kT} - 1 \right) \tag{23}$$

Using Equation (16)–(23), we can calculate the average electron density $\overline{n}$ of an n-type Si nanowire as a function of the nanowire radius r for a given donor density N_{D}, ionization energy N_{I}, interface trap-level density D_{it} and temperature. This is what is shown in Figure 14: $\overline{n}$ as a function of the diameter for various dopant concentrations and a trap-level density $D_{\mathrm{it}} = 1 \times 10^{12}\,\mathrm{eV^{-1}\,cm^{-2}}$. One can see that the average electron density falls off drastically when the diameter is decreased below a certain value, for example, below 25 nm for $N_{\mathrm{D}} = 1 \times 10^{19}\,\mathrm{cm^{-3}}$. This diameter equals $2r_{\mathrm{crit}}$, and it marks the border between the partially depleted and fully depleted nanowires. What is also important to notice in Figure 14, again taking the $N_{\mathrm{D}} = 1 \times 10^{19}\,\mathrm{cm^{-3}}$ as an example, is that even if the nanowire is not fully depleted, for example, at diameters between 30 and 60 nm, the average electron concentration is nevertheless significantly reduced compared to the nominal dopant concentration—an effect presumably caused by the reduced ionization efficiency, as given by Equation (16).

In most cases, a full depletion of the nanowires is mostly unwanted. So the interesting question for the experimentalist is:

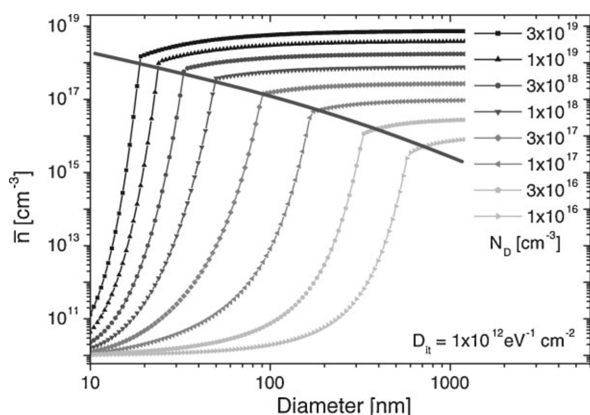

Figure 14. Average electron concentration at 300 K (averaged over the cross-section area) in a Si nanowire as a function of the nanowire diameter, for various donor concentrations N_{d}. The dopant is P with a bulk ionization energy of 45 meV. The interface trap level density $D_{\mathrm{it}} = 1 \times 10^{12}\,\mathrm{eV^{-1}\,cm^{-2}}$.

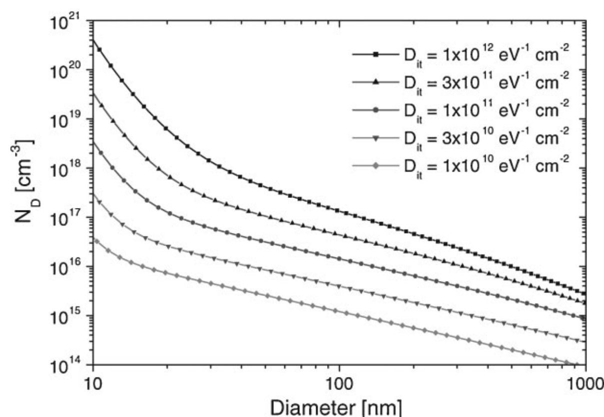

Figure 15. Minimal donor concentration N_{D} necessary to prevent a full depletion of the nanowire. Here given as a function of the nanowire diameter, for various interface trap-level densities D_{it}. The dopant is P with a bulk ionization energy of 45 meV, temperature is 300 K.

what donor concentration (again considering n-type Si only) is necessary to prevent a nanowire of a certain diameter from becoming fully depleted, and how does the concentration change with the quality of the $\mathrm{Si/SiO_2}$ interface, that is, the D_{it} value. This is shown in Figure 15, where the curves are rather straight between 30 and 300 nm. Only for diameters smaller than about 30 nm, a pronounced upward bending can be observed. This upward bending is due to the reduced ionization efficiency at small diameters. It is intuitively understandable that one has to supply some additional dopants to the nanowire in order to compensate for this loss in ionization efficiency. What is also very interesting is that at small diameters the spread between the different curves is larger than the two orders of magnitude by which the D_{it} value is varied. For example, at 20 nm, the necessary donor concentration can be reduced by about three orders of magnitude when the interface trap-level density is reduced by just two orders of magnitude. Therefore, especially at small diameters, it seems that trying to reduce the density of interface states is worthwhile.

A reduction of the interface trap-level density can be achieved by high-temperature annealing, to obtain high-quality oxide, followed by short-time annealing in hydrogen atmosphere to passivate the remaining interface states. D_{it} can in this way be reduced from about $1 \times 10^{12}\,\mathrm{eV^{-1}\,cm^{-2}}$ for a native oxide to values smaller than $1 \times 10^{11}\,\mathrm{eV^{-11}\,cm^{-2}}$.[142] The density of surface charges of Si nanowires has been experimentally determined by Seo et al.[175] and Kimukin et al.,[176] and they found a surface charge density of 2–$3 \times 10^{12}\,\mathrm{cm^{-2}}$ in as-grown Si nanowires. Moreover Seo et al.[175] found that the surface-charge density can be reduced by replacing the native oxide with a high-quality thermal oxide.

4.4. Mobility

The mobility of bulk Si depends on dopant type and concentration. For n-type bulk Si, the electron mobility μ_{e} decreases from about $1500\,\mathrm{cm^2\,Vs^{-1}}$ at $1 \times 10^{15}\,\mathrm{cm^{-3}}$ to about $250\,\mathrm{cm^2\,Vs^{-1}}$ at $1 \times 10^{18}\,\mathrm{cm^{-3}}$.[142] The hole mobility in bulk Si is smaller, and

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

varies between approximately $450\,cm^2\,Vs^{-1}$ at $1\times10^{15}\,cm^{-3}$ and $150\,cm^2\,Vs^{-1}$ at $1\times10^{18}\,cm^{-3}$.[142] The reason why both hole and electron mobilities decrease with increasing impurity concentration is that the ionized impurity atoms act as scattering centers for the charge carriers. Impurity scattering, however, is not the only relevant scattering mechanism. Also phonon scattering plays an important role, in particular at low dopant densities. Considering Si nanowires, also the influence of the nanowire surface on the charge-carrier mobility has to be taken into account, as scattering at the nanowire surface, or at the Si/SiO_2 interface, may have a significant impact.

One can expect that mobility in thin nanowires, with a high surface-to-volume ratio, is reduced due to increased surface scattering. This has been confirmed by simulations that showed that surface scattering becomes dominant in wires smaller than $5\,nm\times5\,nm$, leading to a decrease in the electron mobility with decreasing nanowire cross-section.[177] In these size ranges, phonon scattering also changes. According to Kotlyar et al.,[178] phonon scattering is increased due to an increased overlap between the electron and phonon wavefunction, leading to a degradation of the electron mobility.

Before coming to the mobility of grown Si nanowires, let us, for comparison, take a brief look at mobility determined for horizontal Si nanowires prepared by top-down etching of SOI wafers. Wang et al.[179] measured the mobility in highly p-doped ($10^{18}\,cm^{-3}$) Si nanowires with about $30\,nm\times17\,nm$, and found a mobility of about $100\,cm^2\,Vs^{-1}$, which is close to the mobility in bulk silicon. Gunawan et al.[180] measured the electron and hole mobilities in undoped Si nanowires of $20\,nm\times20\,nm$, and found maximum values of about $370\,cm^2\,Vs^{-1}$ for the electron and $130\,cm^2\,Vs^{-1}$ for the hole mobility.

The mobility of grown silicon nanowires is usually determined by placing nanowires on substrates covered by a thin isolation layer and contacting them at both ends. These contacts then serve as source and drain contacts of a nanowire FET, and a source drain voltage V_{DS} is applied to drive a current through the nanowire. The substrate serves as a back gate, which allows the measuring of the drain–source current I_{DS} as a function of the gate voltage V_G. These data are used to calculate the transconductance $g_m = \partial I_{DS}/\partial V_G$ from which the mobility μ can be obtained, by applying the following formula,[181] originally derived for conventional planar FETs[142]

$$\mu = g_m \frac{L^2}{V_{DS} C} \tag{24}$$

Here, L denotes the device channel length and C the total capacitance. The capacitance C is usually approximated by the oxide capacitance,

$$C_{ox} = \frac{2\pi\varepsilon_{ox}\varepsilon_o L}{\ln(2t_{ox}/r)} \tag{25}$$

This capacitance corresponds to the capacitance of a metallic wire of radius r separated from a metallic gate by an oxide layer of relative permittivity ε_{ox} and thickness t_{ox}. The assumption in Equation (25) of having a metallic wire is important, because it implies that the surface of the wire is taken to be an equipotential surface. This equipotential assumption applied to a cylindrical semiconducting nanowire means to assume a radially symmetric charge-carrier distribution, which, given the asymmetry of the electrostatic problem, is only approximately fulfilled if applying a gate voltage does not lead to too large inhomogeneities in the charge-carrier densities between the side of the wire facing the back-gate and the opposite side. Such a situation may occur when the nanowire radius is too large with respect to the Debye length $L_D = \sqrt{\varepsilon_s\varepsilon_o kT/(q^2 N_B)}$,[142] with N_B being the dopant concentration. Thus, applying equation (25) might be critical for thick semiconducting wires with high dopant concentrations.

Due to the symmetry, this problem does not occur for a surround-gate architecture, where a formula similar to (25) is used for the oxide capacitance.[182] But also in this case, it should be noted that by approximating C by C_{ox}, other capacitances are neglected, such as the depletion-layer capacitance (if present) or the capacitance caused by the interface traps, which do contribute to the total capacitance as well (see ref. [142]). It the total capacitance is given by a serial connection of the oxide capacitance C_{ox} and some parasitic capacitance C_p, then $C^{-1} = C_{ox}^{-1} + C_p^{-1}$. In this case, a reduction of the oxide capacitance, for example by increasing the oxide thickness, would help to minimize the influence of C_p.

The values for the hole mobility, determined in the above-described manner using grown Si nanowires and a backgate, vary strongly. They range from $3\,cm^2\,Vs^{-1}$,[154] considering highly B-doped ($10^{20}\,cm^{-3}$) nanowires, to about $560\,cm^2\,Vs^{-1}$ (peak value $1350\,cm^2\,Vs^{-1}$), for annealed and surface-passivated p-type nanowires.[183] One possible cause for such a high mobility could be a $\langle 110\rangle$ orientation of the nanowires. The authors used nanowires with 10–20 nm diameter,[183] synthesized by a method that, according to an earlier report of the same group, leads to a $\langle 110\rangle$ orientation in this diameter range. Recently, Buin et al.[184] reported that the hole mobility in $\langle 110\rangle$-oriented silicon nanowires is significantly enhanced compared to bulk silicon.

Other authors determined hole mobilities of 325,[181] 119,[185] and $71\,cm^2\,Vs^{-1}$ (peak value $307\,cm^2\,Vs^{-1}$).[186] Ho et al.[187] found an effective electron mobility of $28\,cm^2\,Vs^{-1}$ for a top-gate axially doped ($n^+\ p^-\ n^+$) silicon-nanowire FET. Zheng et al.[188] determined the electron mobility of lightly and heavily *P*-doped nanowires, and found values of $95\,cm^2\,Vs^{-1}$ (peak value $270\,cm^2\,Vs^{-1}$) and $50\,cm^2\,Vs^{-1}$ (peak value $160\,cm^2\,Vs^{-1}$). The hole mobilities reported so far for surround-gated Si nanowire structures are lower, 30[189] and $52\,cm^2\,Vs^{-1}$.[182]

To summarize, there seems to be no simple answer whether mobilities in Si nanowires are larger or smaller than mobilities in bulk Si. According to the data published, both cases seem possible, depending on nanowire diameter, orientation, dopant concentration, and surface quality.

5. Summary and Open Questions

To summarize, we have seen that silicon nanowires can be produced by different growth methods and using a large variety of catalyst materials. Au is the most popular catalyst material, but there are concerns with regard to its defect levels in Si. Considering high-temperature Si-wire growth, some good alternatives to the use of Au exist. Concerning the technologically

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

WILEY InterScience DISCOVER SOMETHING GREAT

important temperature range below 500 °C, however, no real alternative is in sight yet, and it is still an open question whether a good alternative catalyst material can be found. Among the different materials investigated so far, Ag seems to be most promising, but there is definitely need for further investigations. A question in this context that is also unsolved is why catalyst materials such as In or Ga do not work as well as one might expect—whether it is their low Si solubility, their too-low surface tension, or their lack of catalytic ability. A better understanding of the limits of the VLS mechanism would be highly desirable.

Concerning the influence of the surface-tension balance on VLS wire growth, we have seen that the expansion in the initial phase of wire growth and the Nebol'sin stability criterion, a lower limit for the surface tension of the catalyst, can be explained on the basis of simple force-balance relations. These models need to be further developed to allow also for other influence factors, such as growth conditions or the crystallography of the wire. This also holds for the growth velocity of the wires. Although the main consequences of the Gibbs–Thomson effect, which, as we have seen, causes a radius dependence of the growth velocity, are understood at a fundamental level, a thorough understanding of the growth process requires further investigations, concerning in particular the actual level of supersaturation during growth.

With respect to the electrical properties of silicon nanowires, some important factors influencing the resistivity have been discussed. The dielectric confinement causes an increase in the ionization energy and a concomitant decrease in ionization efficiency depending on the radius of the nanowires. In particular for very small nanowires with diameters below 20 nm, the effect is significant, and needs to be taken into account when the electrical properties of nanowires are considered. The second factor that strongly influences the electrical properties are states at the Si/SiO_2 interface, which trap mobile charge carriers and cause a partial or even a full depletion of the nanowire. Simple formulas to estimate the charge-carrier density as a function of nanowire diameter, dopant concentration, and interface trap-level density have been presented. Concerning the mobilities in Si nanowires, it remains unclear whether they are greater or smaller than the mobility in bulk silicon.

Acknowledgements

Thanks to M. Björk for helpful discussion. This work was partially supported by the nanoSTRESS project, the European project NODE (FP6-015783), and the DFG-DIP project GO 704-5 (DIP-K6.1). This article is part of the Special Issue on Nanoionics.

Received: December 18, 2008
Revised: March 4, 2009
Published online: June 2, 2009

[1] R. G. Treuting, S. M. Arnold, *Acta Met.* **1957**, *5*, 598.
[2] R. S. Wagner, W. C. Ellis, *Trans. Met. Soc. AIME* **1965**, *233*, 1053.
[3] D. Zschech, D. H. Kim, A. P. Milenin, R. Scholz, R. Hillebrand, C. J. Hawker, T. P. Russell, M. Steinhart, U. Gösele, *Nano Lett.* **2007**, *7*, 1516.
[4] Y. Zhu, G. S. Cheng, L. D. Zhang, *J. Mater. Sci. Lett.* **1998**, *17*, 1897.
[5] R. S. Wagner, W. C. Ellis, *Appl. Phys. Lett.* **1964**, *4*, 89.
[6] E. I. Givargizov, *J. Cryst. Growth* **1975**, *31*, 20.
[7] A. M. Morales, C. M. Lieber, *Science* **1998**, *279*, 208.
[8] V. A. Nebol'sin, A. A. Shchetinin, *Inorg. Mater.* **2003**, *39*, 899.
[9] S. Kodambaka, J. Tersoff, M. C. Reuter, F. M. Ross, *Phys. Rev. Lett.* **2006**, *96*, 096105.
[10] V. A. Nebol'sin, A. A. Shchetinin, A. A. Dolgachev, V. V. Korneeva, *Inorg. Mater.* **2005**, *41*, 1256.
[11] Y. Wang, V. Schmidt, S. Senz, U. Gösele, *Nat. Nanotechnol.* **2006**, *1*, 186.
[12] S. Akhtar, K. Usami, Y. Tsuchiya, H. Mizuta, S. Oda, *Appl. Phys. Express* **2008**, *1*, 014003.
[13] S. Hofmann, R. Sharma, C. T. Wirth, F. Cervantes-Sodi, C. Ducati, T. Kasama, R. E. Dunin-Borkowski, J. Drucker, P. Bennett, J. Robertson, *Nat. Mater.* **2008**, *7*, 372.
[14] S. Hofmann, C. Ducati, R. J. Neill, S. Piscanec, A. C. Ferrari, J. Geng, R. E. Dunin-Borkowski, J. Robertson, *J. Appl. Phys.* **2003**, *94*, 6005.
[15] S. Sharma, M. K. Sunkara, *Nanotechnology* **2004**, *15*, 130.
[16] F. Iacopi, P. M. Vereecken, M. Schaekers, M. Caymax, N. Moelans, B. Blanpain, O. Richard, C. Detavernier, H. Griffiths, *Nanotechnology* **2007**, *18*, 505307.
[17] Y. Cui, L. H. Lauhon, M. S. Gudiksen, J. Wang, C. M. Lieber, *Appl. Phys. Lett.* **2001**, *78*, 2214.
[18] W. Il Park, G. Zheng, X. Jiang, B. Tian, C. M. Lieber, *Nano Lett.* **2008**, *8*, 3004.
[19] Y. F. Wang, K. K. Lew, T. T. Ho, S. W. Pan, L. Novak, E. C. Dickey, T. S. Redewing, J. M. Mayer, *Nano Lett.* **2005**, *5*, 2139.
[20] L. Pan, K. K. Lew, J. M. Redwing, C. Dickey, *J. Cryst. Growth* **2005**, *277*, 428.
[21] H. Schmid, M. T. Bjork, J. Knoch, H. Riel, W. Riess, *J. Appl. Phys.* **2008**, *103*, 024304.
[22] C. Mouchet, L. Latu-Romain, C. Cayron, E. Rouviere, C. Celle, J. P. Simonato, *Nanotechnology* **2008**, *19*, 335603.
[23] V. Schmidt, S. Senz, U. Gösele, *Nano Lett.* **2005**, *5*, 931.
[24] X.-Y. Zhang, L.-D. Zhang, G.-W. Meng, G.-H. Li, N.-Y. Jin-Phillipp, F. Phillipp, *Adv. Mater.* **2001**, *13*, 1238.
[25] K.-K. Lew, C. Reuther, A. H. Carim, J. M. Redwing, B. R. Martin, *J. Vac. Sci. Tech. B* **2002**, *20*, 389.
[26] T. Shimizu, T. Xie, J. Nishikawa, S. Shingubara, S. Senz, U. Gösele, *Adv. Mater.* **2007**, *19*, 917.
[27] A. V. Sandulova, P. S. Bogoyavlenskii, M. I. Dronyum, *Sov. Phys. Solid State* **1964**, *5*, 1883.
[28] R. S. Wagner, W. C. Ellis, K. A. Jackson, S. M. Arnold, *J. Appl. Phys.* **1964**, *35*, 2993.
[29] E. S. Greiner, J. A. Gutowski, W. C. Ellis, *J. Appl. Phys.* **1961**, *32*, 2489.
[30] T. R. Hogness, T. L. Wilson, W. C. Johnson, *J. Am. Chem. Soc.* **1936**, *58*, 108.
[31] H. Schäfer, B. Morcher, *Z. Anorg. Allg. Chem.* **1957**, *290*, 279.
[32] H. Nagayoshi, H. Nordmark, R. Holmestad, N. Matsumoto, S. Nishimura, K. Terashima, J. C. Walmsley, A. Ulyashin, *Jpn. J. Appl. Phys.* **2008**, *47*, 4807.
[33] Z. W. Pan, Z. R. Dai, *J. Phys. Chem. B* **2001**, *105*, 2507.
[34] Q. Gu, H. Dang, J. Cao, J. Zhao, S. Fan, *Appl. Phys. Lett.* **2000**, *76*, 3020.
[35] F. M. Kolb, H. Hofmeister, R. Scholz, M. Zacharias, U. Gösele, D. D. Ma, S. T. Lee, *J. Electrochem. Soc.* **2004**, *151*, G472.
[36] N. Wang, Y. H. Tang, Y. F. Zhang, D. P. Yu, C. S. Lee, I. Bello, S. T. Lee, *Chem. Phys. Lett.* **1998**, *283*, 368.
[37] N. Wang, Y. H. Tang, Y. F. Zhang, C. S. Lee, I. Bello, S. T. Lee, *Chem. Phys. Lett.* **1999**, *299*, 237.
[38] W. S. Shi, H. Y. Peng, Y. F. Zheng, N. Wang, N. G. Shang, Z. W. Pan, C. S. Lee, S. T. Lee, *Adv. Mater.* **2000**, *12*, 1343.
[39] Y. Shi, Q. Hu, H. Araki, H. Suzuki, H. Gao, W. Yang, T. Noda, *Appl. Phys. A* **2005**, *80*, 1733.
[40] Y. F. Zhang, Y. H. Tang, C. Lam, N. Wang, C. S. Lee, I. Bello, S. T. Lee, *J. Cryst. Growth* **2000**, *212*, 115.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

[41] P. Werner, N. D. Zakharov, G. Gerth, L. Schubert, U. Gösele, *Int. J. Mater. Res.* **2006**, *97*, 1008.
[42] P. Das Kanungo, N. Zakharov, J. Bauer, O. Breitenstein, P. Werner, U. Goesele, *Appl. Phys. Lett.* **2008**, *92*, 263107.
[43] N. D. Zakharov, P. Werner, G. Gerth, L. Schubert, L. Sokolov, U. Gösele, *J. Cryst. Growth* **2006**, *290*, 6.
[44] L. Schubert, P. Werner, N. D. Zakharov, G. Gerth, F. M. Kolb, L. Long, U. Gösele, T. Y. Tan, *Appl. Phys. Lett.* **2004**, *84*, 4968.
[45] Y. F. Zhang, Y. F. Tang, N. Wang, C. S. Lee, I. Bello, S. T. Lee, *Appl. Phys. Lett.* **1998**, *72*, 1835.
[46] G. W. Zhou, Z. Zhang, Z. G. Bai, S. Q. Feng, D. P. Yu, *Appl. Phys. Lett.* **1998**, *73*, 677.
[47] Y.-H. Yang, S.-J. Wu, H. S. Chiu, P.-I. Lin, Y.-T. Chen, *J. Phys. Chem. B* **2004**, *108*, 846.
[48] Y. F. Zhang, Y. H. Tang, H. Y. Peng, N. Wang, C. S. Lee, I. Bello, S. T. Lees, *Appl. Phys. Lett.* **1999**, *75*, 1842.
[49] J. D. Holmes, K. P. Johnston, R. C. Doty, B. A. Korgel, *Science* **2000**, *287*, 1471.
[50] X. M. Lu, T. Hanrath, K. P. Johnston, B. A. Korgel, *Nano Lett.* **2003**, *3*, 93.
[51] T. Hanrath, B. A. Korgel, *Adv. Mater.* **2003**, *15*, 437.
[52] H. Y. Tuan, A. Ghezelbash, B. A. Korgel, *Chem. Mater.* **2008**, *20*, 2306.
[53] A. T. Heitsch, D. D. Fanfair, H. Y. Tuan, B. A. Korgel, *J. Am. Chem. Soc.* **2008**, *130*, 5436.
[54] T. Tezuka, E. Toyoda, S. Nakaharai, N. T. N. Hirashita, N. Sugiyama, Y. Yamashita, O. Kiso, M. Harada, T. Yamamoto, S. Takagi, *IEDM Tech. Dig.* **2007**, 887.
[55] S. F. Feste, J. Knoch, D. Buca, S. Mantl, *Thin Solid Films* **2008**, *517*, 320.
[56] K.-N. Lee, S.-W. Jung, K.-S. Shin, W.-H. Kim, M.-H. Lee, W.-K. Seong, *Small* **2008**, *4*, 642.
[57] S. D. Suk, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D. S. Shin, K. H. Lee, H. S. Park, J. N. Han, C. J. Park, J. B. Park, D. W. Kim, D. Park, B. Ryu, *IEDM Tech. Dig.* **2005**, 717.
[58] S. D. Suk, K. H. Yeo, K. H. Cho, M. Li, Y. Y. Yeoh, S.-Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, C. W. Oh, S. H. Kim, D.-W. Kim, D. Park, *IEEE Trans. Nanotechnol.* **2008**, *7*, 181.
[59] N. Singh, K. D. Buddharaju, S. K. Manhas, A. Agarwal, S. C. Rustagi, G. C. Lo, N. Balasubramanian, D.-L. Kwong, *IEEE Trans. Electron Devices* **2008**, *55*, 3107.
[60] J. R. Heath, *Acc. Chem. Res.* **2008**, *41*, 1609.
[61] L.H.I, D. K. Biegelsen, N. M. Johnson, F. A. Ponce, R. F. W. Pease, *J. Vac. Sci. Technol, B* **1993**, *11*, 2532.
[62] C.-M. Hsu, S. T. Connor, M. X. Tang, Y. Cui, *Appl. Phys. Lett.* **2008**, *93*, 133109.
[63] K. J. Morton, G. Nieberg, S. Bai, S. Y. Chou, *Nanotechnology* **2008**, *19*, 345301.
[64] K.-Q, Peng, Y.-J. Yan, S.-P. Gao, J. Zhu, *Adv. Mater.* **2002**, *14*, 1164.
[65] K. Peng, Z. Huang, J. Zhu, *Adv. Mater.* **2004**, *16*, 73.
[66] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, P. Yang, *Nature* **2008**, *451*, 163.
[67] Z. Huang, H. Fang, J. Zhu, *Adv. Mater.* **2007**, *19*, 744.
[68] Z. Huang, X. Zhang, M. Reiche, L. Liu, W. Lee, T. Shimizu, S. Senz, U. Gösele, *Nano Lett.* **2008**, *8*, 3046.
[69] http://www.britishbiocell.co.uk/.
[70] W. Ostwald, *Lehrbuch der Allgemeinen Chemie*, Vol. *2*, Engelmann, Leipzig, Germany **1896**.
[71] I. M. Lifshitz, V. V. Slyozov, *J. Phys. Chem. Solids* **1961**, *19*, 35.
[72] B. K. Chakraverty, *J. Phys. Chem. Solids* **1967**, *28*, 2401.
[73] P. Wynblatt, N. A. Gjostein, *Acta Met.* **1976**, *24*, 1165.
[74] P. Wynblatt, *Acta Met.* **1976**, *24*, 1175.
[75] A. A. Shchetinin, V. A. Nebol'sin, O. D. Kozenkov, A. F. Tatarenkov, A. I. N. E. P. Dunaev, *Inorg. Mater.* **1991**, *27*, 1137.
[76] J. E. Allen, E. R. Hemesath, D. E. Perea, J. L. Lensch-Falk, Z. Y. Li, F. Yin, M. H. Gass, P. Wang, A. L. Bleloch, R. E. Palmer, L. J. Lauhon, *Nat. Nanotechnol.* **2008**, *3*, 168.
[77] D. E. Perea, J. E. Allen, S. J. May, B. W. Wessels, D. N. Seidman, L. J. Lauhon, *Nano Lett.* **2006**, *6*, 181.
[78] G. A. Bootsma, H. J. Gassen, *J. Cryst. Growth* **1971**, *10*, 223.
[79] Y. Tatsumi, M. Shigi, M. Hirata, *J. Phys. Soc. Jpn.* **1978**, *45*, 703.
[80] Y. Osada, H. Nakayama, M. Shindo, T. Odaka, Y. Ogata, *J. Electrochem. Soc.* **1979**, *126*, 31.
[81] S. J. Whang, S. J. Lee, W. Yang, B. J. Cho, Y. F. Liew, K. Li, L. K. Bera, C. H. Tung, D. L. Kwong, *Conference Abstract 210th ECS Meeting* **2006**, Cancun, Mexico.
[82] S. J. Whang, S. J. Lee, W. F. Yang, B. J. Cho, Y. F. Liew, D. L. Kwong, *Electrochem. Solid-State Lett.* **2007**, *10*, E11.
[83] S. J. Whang, S. J. Lee, D. Z. Chi, W. F. Yang, B. J. Cho, Y. F. Liew, D. L. Kwong, *Nanotechnology* **2007**, *18*, 275302.
[84] J. Bae, N. N. Kulkarni, J. P. Zhou, J. G. Ekerdt, C. K. Shih, *J. Cryst. Growth* **2008**, *310*, 4407.
[85] Y. Miyamoto, M. Hirata, *Jpn. J. Appl. Phys.* **1976**, *15*, 1159.
[86] Y. Yao, S. Fan, *Mater. Lett.* **2007**, *61*, 177.
[87] J. Arbiol, B. Kalache, P. Rocai Cabarrocas, J. R. Morante, A. Fontcuberta i Morral, *Nanotechnology* **2007**, *18*, 305606.
[88] B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, H. A. Atwater, *Appl. Phys. Lett.* **2007**, *91*, 103110.
[89] V. Schmidt, S. Senz, U. Gösele, *Z. Metallkd.* **2005**, *96*, 427.
[90] S. Q. Feng, D. P. Yu, H. Z. Zhang, Z. G. Bai, Y. Ding, *J. Cryst. Growth* **2000**, *209*, 513.
[91] Z. Q. Liu, S. S. Xie, W. Y. Zhou, L. F. Sun, Y. B. Li, D. S. Tang, X. P. Zou, C. Y. Wang, G. Wang, *J. Cryst. Growth* **2001**, *224*, 230.
[92] R. J. Barsotti, J. E. Fischer, C. H. Lee, J. Mahmood, C. K. W. Adu, P. C. Eklund, *Appl. Phys. Lett.* **2002**, *81*, 2866.
[93] E. I. Givargizov, N. N. Sheftal, *J. Cryst. Growth* **1971**, *9*, 326.
[94] M. K. Sunkara, S. Sharma, R. Miranda, G. Lian, E. C. Dickey, *Appl. Phys. Lett.* **2001**, *79*, 1546.
[95] F. Iacopi, O. Richard, Y. Eichhammer, H. Bender, P. M. Vereecken, S. de Gendt, M. Heyns, *Electrochem. Solid-State Lett.* **2008**, *11*, K98.
[96] D. W. F. James, C. Lewis, *Br. J. Appl. Phys.* **1965**, *16*, 1089.
[97] S. Jin, Q. Li, C. S. Lee, *Phys. Status Solidi A* **2001**, *188*, R1.
[98] Y. Tatsumi, M. Hirata, K. Yamada, *J. Phys. Soc. Jpn.* **1981**, *50*, 2288.
[99] J. Weyher, *J. Cryst. Growth* **1978**, *43*, 235.
[100] T. Baron, M. Gordon, F. Dhalluin, C. Ternon, P. Ferret, P. Gentile, *Appl. Phys. Lett.* **2006**, *89*, 233111.
[101] E. C. Garnett, W. Liang, P. Yang, *Adv. Mater.* **2007**, *19*, 2946.
[102] T. I. Kamins, R. S. Williams, Y. Chen, Y.-L. Chang, Y. A. Chang, *Appl. Phys. Lett.* **2000**, *76*, 562.
[103] T. I. Kamins, R. S. Williams, D. P. Basile, T. Hesjedal, J. S. Harris, *J. Appl. Phys.* **2001**, *89*, 1008.
[104] S. Sharma, T. I. Kamins, R. S. Williams, *J. Cryst. Growth* **2004**, *267*, 613.
[105] S. W. Chung, J. Y. Yu, J. R. Heath, *Appl. Phys. Lett.* **2000**, *76*, 2068.
[106] J. Y. Yu, S. W. Chung, J. R. Heath, *J. Phys. Chem. B* **2000**, *104*, 11864.
[107] G. Majni, G. Ottaviani, *Appl. Phys. Lett.* **1977**, *31*, 125.
[108] T. B. Massalski, H. Okamoto, P. Subramanian, L. Kacprzak, in: *Binary Alloy Phase Diagrams*, 2nd Edn, Vol. *1–3*, ASM International, Materials Park, Ohio **1990**.
[109] L. Weber, *Metall. Mater. Trans. A* **2002**, *33A*, 1145.
[110] J. W. Gibbs, in: *The Scientific Papers of J. Williard Gibbs, PH.D, LL.D, Vol. I. Thermodynamics*, Longmans, Green, and Co., London, New York, Bombay **1906**, pp. 315–318.
[111] R. Shuttleworth, *Proc. Phys. Soc. A* **1950**, *63*, 444.
[112] J. W. Cahn, *Acta Met.* **1980**, *28*, 1333.
[113] J. W. Gibbs, in: *The Scientific Papers of J. Williard Gibbs, PH.D, LL.D, Vol. I. Thermodynamics*, Dover Publications, New York **1961**, pp. *287–288*, Ch. 3.
[114] J. S. Rowlinson, B. Widom, in: *Molecular Theory of Capillarity*, Dover Publications, Mineola, NY **2002**, p. 209, Ch. 3.
[115] J. Weyher, *Mater. Sci. Eng.* **1975**, *20*, 171.
[116] A. A. Shchetinin, B. M. Darinskii, O. D. Kozenkov, V. A. Nebol'sin, *Inorg. Mater.* **1990**, *26*, 1157.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim
WILEY InterScience DISCOVER SOMETHING GREAT

[117] Y. Wakayama, S. Tanaka, *Surf. Sci.* **1999**, *420*, 190.
[118] E. I. Givargizov, *Highly Anisotropic Crystals*, Reidel, Dordrecht **1987**.
[119] B. Ressel, K. C. Prince, S. Heun, Y. Homma, *J. Appl. Phys.* **2003**, *93*, 3886.
[120] G. A. Satunkin, V. A. Tatarchenko, *Kristallografiya* **1985**, *30*, 772.
[121] Y. A. Tatarchenko in, *Shaped Crystal Growth*, Kluwer Academic, Dordrecht **1993**, pp. 197–206, Ch. 1.
[122] V. Schmidt, S. Senz, U. Gösele, *Appl. Phys. A* **2005**, *80*, 445.
[123] J. S. Rowlinson, B. Widom, *Molecular Theory of Capillarity*, Dover Publications, Mineola, NY **2002**.
[124] P. Chen, J. Gaydos, A. W. Neumann, *Langmuir* **1996**, *12*, 5956.
[125] Y. V. Naidich, V. M. Perevertailo, L. P. Obushchak, *Zh. Fiz. Khim.* **1975**, *49*, 1554.
[126] R. J. Jaccodine, *J. Electrochem. Soc.* **1963**, *110*, 524.
[127] S. C. Hardy, *J. Cryst. Growth* **1985**, *71*, 602.
[128] M. Demeri, M. Farag, J. Heasley, *J. Mater. Sci. Lett.* **1974**, *9*, 683.
[129] W. L. Falke, A. E. Schwaneke, R. W. Nash, *Metall. Trans. B* **1977**, *8B*, 301.
[130] D. Giuranno, F. Gnecco, E. Ricci, R. Novakovic, *Intermetallics* **2003**, *11*, 1313.
[131] W. Gasior, Z. Moser, J. Pstrus, *J. Phase Equilib.* **2003**, *24*, 504.
[132] M. A. McClelland, J. S. Sze, *Surf. Sci.* **1995**, *330*, 313.
[133] K.-K. Lew, J. M. Redwing, *J. Cryst. Growth* **2003**, *254*, 14.
[134] Y. Wu, R. Fan, P. Yang, *Nano Lett.* **2002**, *2*, 83.
[135] J. Kikkawa, Y. Ohno, S. Takeda, *Appl. Phys. Lett.* **2005**, *86*, 123109.
[136] H. Schmid, M. T. Björk, J. Knoch, S. Karg, H. Riel, W. Riess, *Nano Lett.* **2009**, *9*, 173.
[137] V. Schmidt, S. Senz, U. Gösele, *Phys. Rev. B* **2007**, *75*, 045335.
[138] T. Y. Tan, N. Li, U. Gösele, *Appl. Phys. Lett.* **2003**, *83*, 1199.
[139] T. Y. Tan, N. Li, U. Gösele, *Appl. Phys. A* **2004**, *78*, 519.
[140] F. Dhalluin, P. J. Desré, M. I. den Hertog, J. Rouvière, P. Ferret, P. Gentile, T. Baron, *J. Appl. Phys.* **2007**, *102*, 094906.
[141] J. B. Hannon, S. Kodambaka, F. M. Ross, R. M. Tromp, *Nature* **2006**, *440*, 69.
[142] S. M. Sze, in: *Physics of Semiconductor Devices*, 2nd Edn., Wiley, New York **1981**.
[143] J.-M. Zhang, F. Ma, K.-W. Xu, X.-T. Xin, *Surf. Interface Anal.* **2003**, *35*, 805.
[144] P. M. Fahey, P. B. Griffin, J. D. Plummer, *Rev. Mod. Phys.* **1989**, *61*, 289.
[145] H. Peelaers, B. Partoens, F. M. Peeters, *Nano Lett.* **2006**, *6*, 2781.
[146] V. Schmidt, H. Riel, S. Senz, S. Karg, W. Riess, U. Gösele, *Small* **2006**, *2*, 85.
[147] Y. H. Tang, T. K. Sham, A. Jürgensen, Y. F. Hu, C. S. Lee, S. T. Lee, *Appl. Phys. Lett.* **2002**, *80*, 3709.
[148] N. Fukata, J. Chen, T. Sekiguchi, N. Okada, K. Murakami, T. Tsurui, S. Ito, *Appl. Phys. Lett.* **2006**, *89*, 203109.
[149] N. Fukata, J. Chen, T. Sekiguchi, S. Matsushita, T. Oshima, N. Uchida, K. Murakami, T. Tsurui, S. Ito, *Appl. Phys. Lett.* **2007**, *90*, 153117.
[150] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, C. M. Lieber, *Nature* **2002**, *415*, 617.
[151] C. Yang, Z. Zhong, C. M. Lieber, *Science* **2005**, *310*, 1304.
[152] E. I. Givargizov, *J. Cryst. Growth* **1973**, *20*, 217.
[153] K.-K. Lew, L. Pan, T. E. Bogart, S. M. Dilts, E. C. Dickey, J. M. Redwing, Y. F. Wang, M. Cabassi, T. S. Mayer, S. W. Novak, *Appl. Phys. Lett.* **2004**, *85*, 3101.
[154] Y. Cui, X. Duan, J. Hu, C. M. Lieber, *J. Phys. Chem. B* **2000**, *104*, 5213.
[155] R. T. White, R. L. Espino-Rios, D. S. Rodgers, M. A. Ring, H. E. O'Neal, *Int. J. Chem. Kinet.* **1985**, *17*, 1029.
[156] J. M. Jasinski, S. M. Gates, *Acc. Chem. Res.* **1991**, *24*, 9.
[157] M. Diarra, Y. M. Niquet, C. Delerue, G. Allan, *Phys. Rev. B* **2007**, *75*, 045301.
[158] Y. M. Niquet, A. Lherbier, N. H. Quang, M. V. Fernandez-Serre, X. Blase, C. Delerue, *Phys. Rev. B* **2006**, *73*, 165319.
[159] M. Diarra, C. Delerue, Y. M. Niquet, G. Allan, *J. Appl. Phys.* **2008**, *103*, 073703.
[160] M. T. Björk, H. Schmid, J. Knoch, H. Riel, W. Riess, *Nat. Nanotechnol.* **2009**, *4*, 103.
[161] B. E. Deal, *IEEE Trans. Electron Devices* **1980**, *ED-27*, 606.
[162] M. H. White, J. R. Cricchi, *IEEE Trans. Electron Devices* **1972**, *ED-19*, 1280.
[163] Y. Nishi, *Jpn. J. Appl. Phys.* **1966**, *5*, 333.
[164] Y. Nishi, *Jpn. J. Appl. Phys.* **1971**, *10*, 52.
[165] Y. Nishi, A. Ohwada, K. Tanaka, *Jpn. J. Appl. Phys.* **1972**, *11*, 85.
[166] D. L. Griscom, *Phys. Rev. B* **1980**, *22*, 4192.
[167] P. J. Caplan, E. H. Poindexter, B. E. Deal, R. R. Razouk, *J. Appl. Phys.* **1979**, *50*, 5847.
[168] P. M. Lenahan, P. V. Dressendorfer, *Appl. Phys. Lett.* **1982**, *41*, 542.
[169] P. M. Lenahan, P. V. Dressendorfer, *J. Appl. Phys.* **1983**, *54*, 1457.
[170] P. M. Lenahan, P. V. Dressendorfer, *Appl. Phys. Lett.* **1984**, *44*, 96.
[171] Y. Y. Kim, P. M. Lenahan, *J. Appl. Phys.* **1988**, *64*, 3551.
[172] N. M. Johnson, D. K. Biegelsen, M. D. Moyer, S. T. Chang, E. H. Poindexter, P. J. Caplan, *Appl. Phys. Lett.* **1983**, *43*, 563.
[173] E. H. Poindexter, P. J. Caplan, B. E. Deal, R. R. Razouk, *J. Appl. Phys.* **1981**, *52*, 879.
[174] V. Schmidt, S. Senz, U. Gösele, *Appl. Phys. A* **2007**, *86*, 187.
[175] K. I. Seo, S. Sharma, A. A. Yasseri, D. R. Stewart, T. I. Kamins, *Electrochem. Solid-State Lett.* **2006**, *9*, G69.
[176] I. Kimukin, M. S. Islam, R. S. Williams, *Nanotechnology* **2006**, *17*, S240.
[177] E. B. Ramayya, D. Vasileska, S. M. Goodnick, I. I. Knezevic, *J. Appl. Phys.* **2008**, *104*, 063711.
[178] R. Kotlyar, B. Obradovic, P. Matagne, M. Stettler, M. D. Giles, *Appl. Phys. Lett.* **2004**, *84*, 5270.
[179] D. Wang, B. A. Sheriff, J. R. Heath, *Nano Lett.* **2006**, *6*, 1096.
[180] O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight, S. Guha, W. Haensch, *Nano Lett.* **2008**, *8*, 1566.
[181] Y. Wu, J. Xiang, C. Yang, W. Lu, C. M. Lieber, *Nature* **2004**, *430*, 61.
[182] J. Goldberger, A. I. Hochbaum, R. Fan, P. Yang, *Nano Lett.* **2006**, *6*, 973.
[183] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, C. M. Lieber, *Nano Lett.* **2003**, *3*, 149.
[184] A. K. Buin, A. Verma, A. Svizhenko, M. P. Anantram, *Nano Lett.* **2008**, *8*, 760.
[185] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, J. L. Goldman, *Nature* **2003**, *425*, 274.
[186] S. Jin, D. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, C. M. Lieber, *Nano Lett.* **2004**, *4*, 915.
[187] T.-T. Ho, Y. Wang, S. Eichfeld, K.-K. Lew, B. Liu, S. E. Mohney, J. M. Redwing, T. S. Mayer, *Nano Lett.* **2008**, *8*, 4359.
[188] G. Zheng, W. Lu, S. Jin, C. M. Lieber, *Adv. Mater.* **2004**, *16*, 1890.
[189] M. T. Björk, O. Hayden, H. Schmid, H. Riel, W. Riess, *Appl. Phys. Lett.* **2007**, *90*, 142110.
[190] M. T. Björk, J. Knoch, H. Schmidt, H. Riel, W. Riess, *Appl. Phys. Lett.* **2008**, *92*, 193504.
[191] L. J. Lauhon, M. S. Gudiksen, D. Wang, C. M. Lieber, *Nature* **2002**, *420*, 57.

© 2009 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim