CLASSIFICATION OF SHUNTING MECHANISMS IN CRYSTALLINE SILICON SOLAR CELLS

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Abstract The efficiency of a solar cell is given by its average electrical parameters. On inhomogeneous materials and especially on large-area solar cells the inhomogeneity of the short circuit current, the open circuit voltage and the fill factor are important factors to reach high and stable efficiencies and may limit the overall performance of the device.

A locally increased dark forward current (shunt) reduces the fill factor and the open circuit voltage of the whole cell. The inhomogeneity of the forward current in a solar cell can be measured using lock-in thermography. The quantitative and voltage-dependent evaluation of these thermographic investigations of various solar cell types on mono- or multicrystalline silicon enables the

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classification of the different shunting mechanisms found. By further microscopic investigations the physical reasons for the increased dark forward currents can be determined.

It turns out that a high density of crystallographic defects like dislocation tangles or microdefects can be responsible for an increased dark forward current. Unexpectedly, grain boundaries in solar cells on multicrystalline silicon do not show any measurable influence on the local dark forward current. In most cases shunts caused by process-induced defects are dominating the current-voltage characteristic at the maximum power point of the solar cell. In commercial solar cells shunts at the edges are most important, followed by shunts beyond the grid lines.

1. Introduction

The performance of a solar cell is determined by its integral open circuit voltage U_{OC}, the short circuit current I_{SC} and the fill factor FF. Due to the large area of solar cells, the inhomogeneous materials used and the cost effective solar cell processes these parameters may vary strongly over the cell area. Therefore the investigation of the local electrical behavior of the cell parameters is an important tool in the understanding and quantification of the different loss mechanisms in solar cells. This is commonly done for the local short circuit current with the LBIC (light beam induced current) technique in measuring the short circuit current under local illumination [1]. Under applied bias the different parts of the cell act in parallel, and the extraction of the local information out of the electrical signal is no longer possible. Of course it is possible to create an array of small single diodes covering the surface [1,2] and to measure their IV-characteristic separately. But this requires a special preparation technique and excludes important parts of the standard cell as e.g. the edges and the grid. In most cases - if the series resistance can be neglected - the illuminated IV-characteristic is given in good aproximation by the superposition of the dark IV-characteristic and

the photocurrent. Thus any inhomogeneities of the forward current appears already without illumination if an appropriate voltage is applied to the solar cell. Under applied bias any current flow is governed by a dissipation of power and thus a leakage current leads to an increased temperature. Therefore inhomogeneities in the fill factor and the open circuit voltage can be imaged by thermography, as was first demonstrated by Simo and Martinuzzi [3]. The short term "shunt" is used here for any locally enhanced injection current even if not a hard shunt exists, which would lead to a short in the cell and a complete failure of the device. Hard shunts are most likely due to misalignment if e.g. a metallization line extends around the edge of the cell; they are out of the focus of this contribution. In most cases of interest the leakage current is not that high and therefore the thermal signal is weak and cannot be measured with conventional stationary thermography. The improved sensitivity of lock-in thermography enables the measurement of these shunts, and their quantitative influence on the solar cells efficiency can be calculated. With lock-in thermography either as contact thermography [4] or IR thermography [5] a few hundred solar cells on crystalline silicon have been investigated up to now. Different types of shunts have been reported, some of them seem to be typical and some of them belonging to a specific material or solar cell process. In this contribution an overview about the typical shunting mechanisms found in crystalline silicon solar cells is given.

2. Lock-in thermography

The local heating under bias is proportional to the local dissipated power, itself being proportional to the local current if a fixed voltage is applied. Thus thermography enables the local current measurement under external bias. In order to increase the thermal and the lateral resolution it is possible to apply the bias voltage periodically and to measure the temperature modulation in the

lock-in mode. Part of the experiments presented here were done using DPCT (dynamic precision contact thermography [4]) with a thermistor in thermal contact with the solar cell and a mechanical scanning system. More elegant, much faster, and without mechanical contact this can also be done using a commercial FPA (focal plane array) infrared camera in performing an online digital lock-in correlation of the whole images in a fast computer. Thus the digital lock-in correlation is done numerically independently for each pixel and the increased signal/noise ratio is achieved without any smoothing keeping the original lateral resolution of the image. These investigations with an IR camera were done either by using a InSb based detector with 128*128 pixel by AMBER Inc. [5] or using a MCT (mercury cadmium telluride) detector with 384*288 pixels by Thermosensorik GmbH [6]. Technical details and a description of the digital lock in procedure are given elsewhere [4,5]. In the following the experimental results will be presented together independently of the setup they are measured with, since there is no principal difference between DPCT or lock-in IR thermography. A very detailed discussion of the technique and the advantages and disadvantages of these systems will be given in [7]. For the IR-camera based systems a noise level of 10 µK (r.m.s) is achievable typically within one hour integration time. Solar cells of any size and using a microscope objective structures down to 10 µm can be investigated.

In order to be able to estimate the importance of the shunts found under normal working conditions of the solar cell, a bias voltage close to the working point of the cell should be chosen. In most cases presented here 0.5 V forward bias were used. The lock-in thermography can be analyzed quantitatively, since the local temperature modulation is proportional to the dissipated power [4,7]. Techniques were developed for the extraction of the shunt strength out of the quadrature signal [8]. The impact of single shunts on the IV-characteristic and hence on the efficiency can be calculated from a series of thermograms at different voltages. Since thermography is not an analytical method,

further investigations using e.g. optical or electron-microscopy, EBIC, EDX analysis or SIMS have to be used to identify the physical reason of the shunts.

3. Typical shunts in crystalline silicon solar cells

Using lock-in thermography a whole lot of different shunts have been reported in solar cells on different materials. Shunts at the outer edges in solar cells on multi- [9,10] and monocrystalline [4] silicon, on silicon sheets [8], as well as after laser scribing [11] have been reported. Point shunts on the surface beyond the grid [10,12,13] and in the uncovered emitter [10,14] could be found. Some reasons for shunts are easily fixed if a large scratch on the surface is correlated to the shunt or the already soldered string contact can be seen in the thermography [15]. Additionally there are often broad features in the lock-in thermograms of solar cells on mc-silicon which are not as localized as these point or line shunts. They appear as weak cloudy background and seem to be correlated to the grain structure. An example will be given in chapter 3.2. Surprisingly, up to now no grain boundaries could ever be found to be responsible for a locally enhanced current injection by lock-in thermography. In the following some examples of shunts in solar cells on mono- and multi-crystalline silicon will be presented.

3.1 Shunts in solar cells on Czochralski silicon

Figure 1 shows a thermogram of a 10*10 cm² solar cell on Czochralski silicon with a diffused emitter. The strongest shunt in this cell is beyond a major grid line. Additionally there are shunts at the edges of this cell due to the insufficient passivation here. After longer measurement time and reaching a noise level of 10 to 20 μK a weak, broadened double ring structure appears in the thermogram. It is caused by the point defect clusters incorporated into the material during the fast

growth process often used for solar grade Cz-silicon. A quantitative analysis shows that the main shunt is responsible for an extra leakage current of 10 mA at the 0.5 Volts used in Fig. 1. The edge shunts contribute with aprox. 22 mA, whereas the defects in the broad ring structure all together carry a leakage current of 150 mA at 0.5 Volt.

3.2. Shunts in multicrystalline silicon solar cells

Figure 2 shows a typical thermogram of a commercial 100 cm² solar cells on block cast multicrystalline silicon. The image shows an increased heating at the outer edges of the solar cell with the main shunt in one corner. These shunts are caused by an insufficient separation of the emitter from the rear contact, being obviously problematic in different technologies. They give a thermal signal of a few millikelvin and are already visible after a few seconds measurement time. The main shunt in Fig.2 is caused by a broken corner of the wafer and an insufficient edge treatment here. Edges of processed solar cells broken after the cell process induces only weak leakage currents (see e.g. upper right corner of Fig.1). Despite of a few additional point shunts on the surface broad but weak temperature modulations can be found on the whole wafer. They are in good correlation with the regions of reduced carrier lifetime found in LBIC (Fig. 3). A quantitative evaluation reveals the current caused by these defects being with 20 mA at 0.5 Volt in the same range as the leakage current caused by the edge shunts in this sample (25 mA). For the area marked in Fig. 3 an increased current density of about 1 mA caused by these defects can be calculated. With a dislocation density of $5*10^5$ cm^{-2} this corresponds to an average leakage current in the range of 0.2 .. 1 nA per dislocation in this example, being in good agreement with calculations of El Ghitani and Martinuzzi.

4. Classification of shunts

Common to all commercial cells not using planar technology are edge shunts. Their quantitative influence depends of course on the technology used, but they are often among the stronger shunts. They are due to the insufficient separation of the diffused emitter from back contacts. The second important contribution are shunts beyond the emitter contacts. These shunts may be caused e.g. by spots of missing emitter or mechanical damage of the diffused surface. These shunts are most likely showing an electrical behaviour of a Schottky contact. In solar cells made on very uneven surfaces as e.g. polycrystalline silicon with humps on the substrate [12] or silicon crystallized in thin sheets, the emitter formation might be incomplete if an overhang exists at a hump, leading to strong shunts if a grid line covers this area (see Fig. 4). Relatively rarely point like shunts in the emitter beside the grid lines can be found. They may be caused by precipitates incorporated in the silicon material [10].

All localized shunts discussed above cause local temperature modulations above 100 µK and can be measured within minutes. Since the leakage current caused by a single crystal defect is very small, only high defect densities with nevertheless very weak temperature signal can be detected. This is shown here for dislocations in block cast silicon and for grown-in defect clusters in solar grade Cz-silicon.

5. Conclusion

In nearly all solar cells on crystalline silicon locally increased leakage currents can be found. They vary, depending on the material and process involved, in their strength and frequency. The quantification of their influence is important for the development and control of a solar cell process.

Their localization and electrical characterization with lock-in thermography is the presupposition for a detailed analysis with other techniques.

In detailed investigations a contribution of crystal defects can be found. Despite the very weak temperature signal height caused by these kind of defects, their high number giving broad signals in the thermogram may be responsible for an important contribution to the leakage current. Of course, the recombinative properties of these defects can be tracked much easier in LBIC and lifetime measurements.

Contrary to all expectations no influence of the grain structure on the thermograms could be found. Thus there seems to be no remarkable disturbance of the pn-junction at the grain boundaries, and their recombinative contribution to the leakage current seems to be weak.

Thus, even if the strongest point shunts in typical cells causing a local temperature signal around one millikelvin in solar cells around 15% efficiency are measurable within seconds, the detailed analysis including extended defect areas may require a measurement time of several hours.

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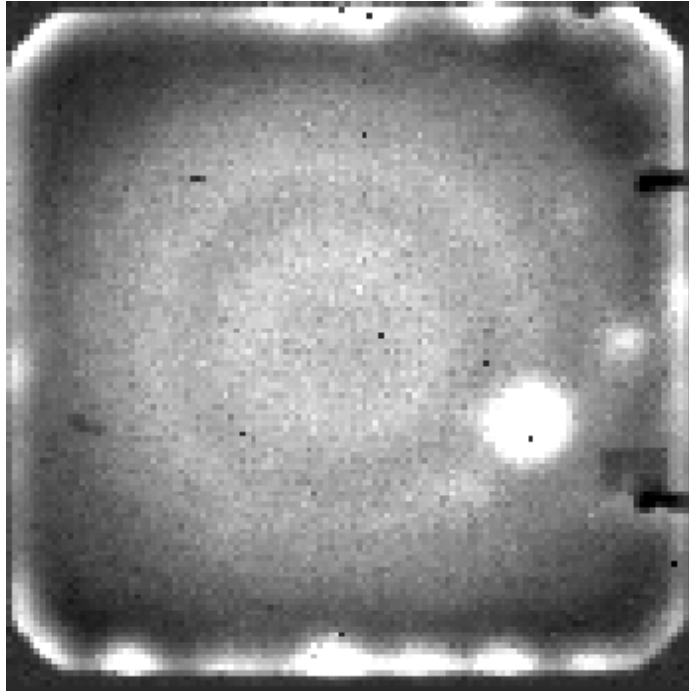
EMRS 2001, E5.7 **Figure Captions**

Fig. 1: Lock-in thermogram of a 10*10 cm² solar cell on Cz-silicon. Temperatur modulation from 0 to 0.15 mK, the main shunt and the edge shunts appear broadened since they are out of scale.

Fig. 2: Lock-in thermogram of a solar cell (10*10 cm²) on multicrystalline silicon at 10 Hz and 0.5 Volt forward bias. Temperature modulation scale from 0..0.25 mK. The main shunt in the upper left corner is out of scale.

Fig. 3: Detail of Fig. 2 with an increased temperature scale (left). The weak broad areas of increased leakage current (bright) in the thermogram correlate well with the dark regions if decreased electron lifetime resulting in a decreased short circuit current in the LBIC image on the right.

Fig. 4: Hump in the structure of a thin crystalline silicon layer on a substrate (SE image at 10 kV) giving a strong shunt if covered with the emitter grid [12]. The diameter of this silicon sphere exceeds the thickness of the silicon layer. The straight line is the border of the metallization.
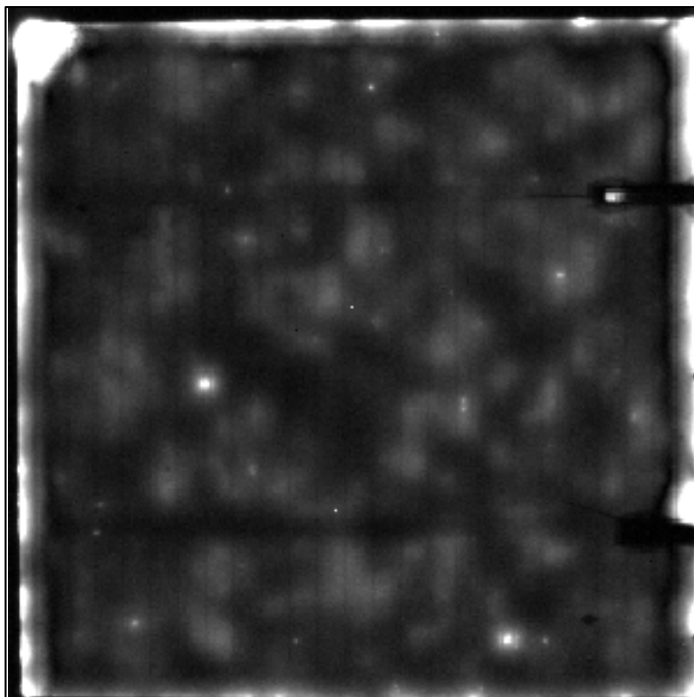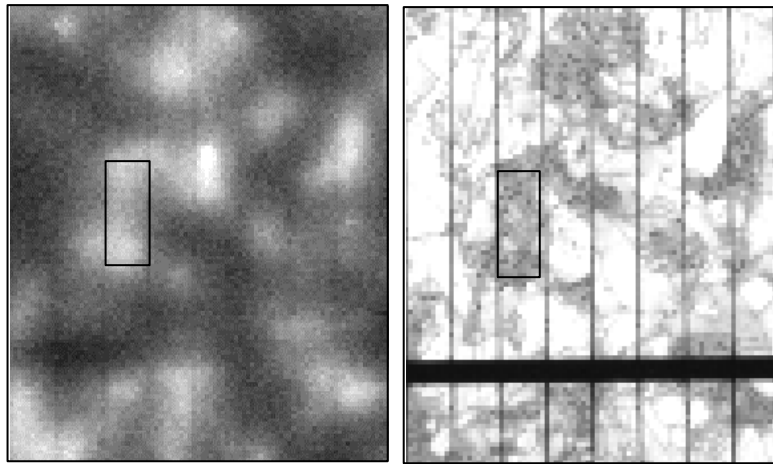
EMRS 2001, E5.7 Figure 3

EMRS 2001, E5.7 Figure 4