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Application of lock-in thermography for failure analysis in integrated circuits using quantitative phase shift analysis

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ABSTRACT

Lock-in thermography (LIT), which is a well established technique for non-destructive evaluation, can also be used to identify and locate thermal active electrically defects like shorts and resistive opens in microelectronic devices. Defect localization on the level of the integrated circuits (IC) requires a μm resolution. But LIT can also be applied to locate buried thermal active defects within fully packaged microelectronic devices by analysing the thermal signal detected at the surface of the device. In addition to the lateral localization of the hot spot, its depth can also be determined by analysing the phase shift of the thermal signal. This is especially valued for non destructive defect localization in complex 3D integrated system in package devices (3D SiP). In comparison to competitive thermal imaging techniques, like liquid crystal imaging or fluorescent micro thermal imaging, LIT is easier to apply since it does not need any foreign thermal sensitive layer at the surface of the device. Also, the sensitivity limit of this technique within μK range is significantly better. In addition the dynamic character of LIT reduces thermal blurring, and the problem of inhomogeneous IR emissivity can be overcome by using the phase image or the $0^\circ/-90^\circ$ image. The spatial resolution limit of the used microscopic thermal imaging setup performed in the mid-wavelength range is about 5 μm, but can be improved to 1.5 μm by applying solid immersion lenses. Within the paper, the principle theory of LIT and the practical use for both, single and multiple IC devices is presented.

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1. Introduction

Since many years the complexity of microelectronic devices steadily increases and the dimension and power consumption of their basic elements (transistors etc.) steadily reduces. According to this trend failure analysis (FA) is an increasingly demanding challenge. Defects could be built in as structural weaknesses during device fabrication or could be caused by electrical overstress during operation. The task of FA is to look for root causes of such failures in order to improve fabrication processes and to increase reliability and robustness of the devices. Many of the possible faults in microelectronic devices are connected with local heat dissipation, such as electrical shorts, oxide or junction breakdowns, high resistive opens, latch-ups, and many more. Therefore, besides microscopic techniques light microscopic thermography methods are widely used for localizing such defects within the complex wiring of the device. In the last decades, the most popular micro-thermography methods were liquid crystal (LC) microscopy [1], fluorescent micro thermal imaging (FMI) [2], and steady-state thermal infrared microscopy [3]. The latter method seems to be the most elegant one, since, in contrast to the other methods; it does not need to apply any foreign layer at the surface. However, here the microscopic image is given by the product of IR irradiation (associated to the temperature increase) and emissivity ε, which may be between 0.01 and 1. On reflecting surfaces like metallization ε is below 0.1, but on black surfaces it approaches 1. Correcting this so-called emissivity contrast is possible, but experimentally demanding and time-consuming [3]. The temperature resolution of all these previous thermography techniques is in the order of 0.1 K. However, many faults are leading to very small temperature signals in the order of 1 mK or less. Therefore, steady-state thermography techniques were only able to detect relatively strong heat sources above the threshold of 100 mK. Moreover, in the investigated device the heat naturally tends to spread away laterally. This leads to a very blurred appearance of thermal images, even if the heat sources are very local. Especially for the application of defect localization at microelectronic devices, the resulting spatial resolution of micro-thermography is often not sufficient. There are

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a number of laser-based thermographic techniques like internal infrared laser deflection or transmission Fabry–Perot interference thermometry [4,5]. Since these techniques are sequentially scanning and require a quite complex setup, they have not become popular in thermal failure analysis yet.

Lock-in thermography (LIT) works on the principle that heat sources are periodically intensity-modulated at a certain lock-in frequency and that only the local temperature modulation is evaluated according to the lock-in principle and averaged over many lock-in periods [6]. Since the last decade, LIT is used systematically for FA on ICs [7]. Due to the dynamic nature of LIT, the lateral heat diffusion is widely suppressed, hence the effective spatial resolution is improved. Due to the averaging nature of LIT, after a certain acquisition time (typically some minutes), tiny temperature modulations in the order of 0.1 mK can be detected. This has lead to a strong expansion of the application field of thermal analysis in microelectronic FA. Since LIT two-channel lock-in correlation is used, the phase image can be displayed where the emissivity contrast is inherently compensated. This phase information can be further used for investigating the device internal heat propagation. Although the direct optical access to the defective area is blocked by opaque material layers, heat can propagate through these layers resulting in a local temperature variation at the device surface. This propagation process is time-depending and in consequence creates a phase shift between excitation signal and detected thermal response. Knowing the internal structure and the thermal properties of the device under test, the quantitative phase shift determination can be used for defect depth allocations. This information in combination with lateral defect localization enables non destructive defect localization within all three dimensions. This approach was successfully demonstrated on test samples in [8] and real devices [9]. Furthermore, previous works have treated theoretically such kind of measurements in ICs [10].

More recently, CCD-based thermoreflectance microscopy has appeared as another useful microthermal inspection method [11]. Here the property of any reflection coefficient to depend on temperature is used. Like LIT, this method is working in lock-in mode, leading to an improved sensitivity and spatial resolution. Due to the lower wavelength used for imaging, its spatial resolution is superior to LIT. However, due to the low temperature coefficients of the reflection (in the order of 10^{-4}/K) the detection limit of thermoreflectance microscopy is well below that of LIT.

2. Theory of heat propagation

LIT bases on the principle theory of thermal wave propagation which are generated as a cause of a harmonic temperature excitation [12]. Therefore, heat propagation through an opaque layer is depending on the angular stimulation frequency, distance of the buried defect to the surface and the thermal parameters of the propagated material layers. Considering a semi-infinite body of the thickness z which surface temperature is a harmonic signal function with the angular frequency ω, the resulting temperature signal can be regarded and calculated as a "thermal wave" by the expression:

$$T(z) = A \cdot \sin(\omega t - \varphi) \tag{1}$$

with A as the amplitude:

$$T_{z=0} \cdot e^{-z/\mu} \tag{2}$$

and φ representing the phase of the wave:

$$\varphi = \frac{z}{\mu} = \frac{z}{\sqrt{2a/\omega}} \tag{3}$$

The parameter which describes the influence of the thermal properties of a material layer is named as thermal diffusion length (μ) and

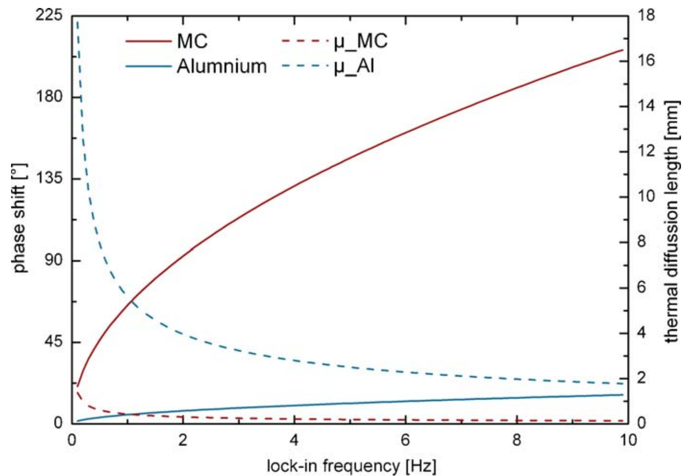

Fig. 1. Phase shift vs. frequency relationship for buried defects under an opaque layer of aluminium (blue) and MC (red). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of the article.)

defines the damping of the thermal wave inside of a bulk material. It can be calculated by knowing heat conductivity (λ in W/m K), specific heat capacity (c_p in J/g K), density (ρ in g/cm^3) and the applied lock-in frequency ($f_{\text{lock-in}}$ in Hz). The thermal parameters of the material can be summarized as the thermal diffusivity (a in mm^2/s):

$$a = \frac{\lambda}{c_p \cdot \rho} \tag{4}$$

Investigating buried heat sources in opaque materials, the thermal diffusion length can be seen as the damping factor to the thermal wave which affects both amplitude and phase signal. Higher lock-in frequencies results in a stronger delay between excitation signal at the defect position and the thermal response at the device surface. Therefore, an increase of the phase shift as a function of the increased lock-in frequency can be regarded. Fig. 1 shows the resulting phase shift vs. frequency relationship for assumed buried defects under 500 μm mould compound and aluminium layer. Both materials are considered as opaque.

The fact that the resulting phase shift depends on both thermal diffusion length and geometrical thickness can be used for a "fingerprint" determination of hot spots depths within multi-layer devices, Fig. 2.

Depending on the defect depth, heat has to propagate through different numbers of material layers before reaching the device surface. Each opaque layer contributes a discrete value to the overall phase shift. Hence, knowing these values buried defects can be located within the layer stack by measuring the overall phase shift. Knowing the thermal behaviour of each layer the phase shifts contributions can be calculated. Alternatively the phase shift values can be experimentally determined at reference devices by removing each layer step by step and measuring the corresponding phase shift for the residual layer stack. As an example, stacked die devices

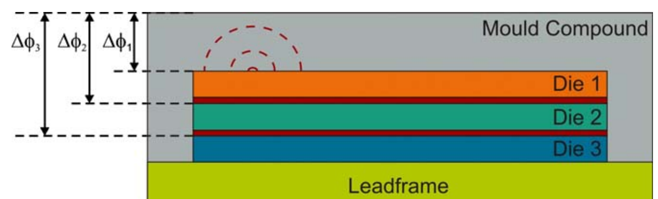

Fig. 2. Simplified sketch of a stacked die device and illustration of the resulting phase shift values per defect depths.

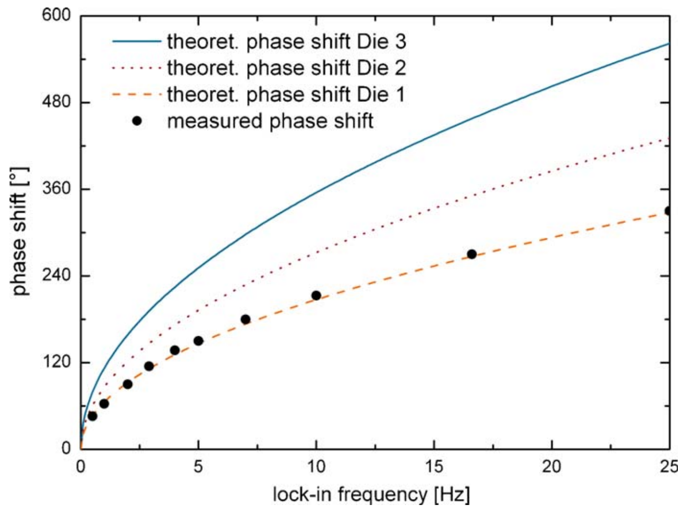

Fig. 3. Calculated phase shift signals of each die level within a stacked die device and comparison to measured phase shift values.

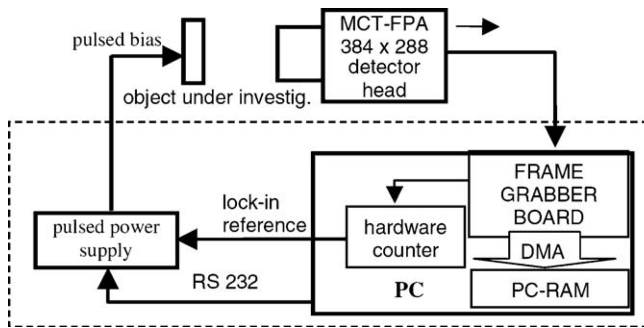

Fig. 4. Block scheme of a typical LIT system.

containing Si dies with an adhesive layer in between. This IC stack is encapsulated by a mould compound (MC). Because Si is transparent to IR only each adhesive layer and the MC layer above contributes to the phase shift, Fig. 3.

3. Experimental setup of LIT

For experiments, the LIT system Thermosensorik TDL 640XL is used. Fig. 4 shows the scheme of a typical LIT system. An IR camera with a pixel resolution of 640 by 512 pixels (pixel pitch ∼ 15 μm) is running at a certain frame rate (100 Hz), and the frame trigger is fed to a programmable frequency divider (counter) which generates the lock-in trigger. This triggers a pulsed power supply (in this case an Agilent 6700B) which modulates the supply current of the device under test. The thermo-camera is usually a mid-wave one (3–5 μm) since the long-wave cameras (8–10 μm) show a degraded diffraction-limited spatial resolution. Fig. 5 shows the principle of the 2-phase lock-in correlation. In two separate logical channels, the incoming IR images are multiplied by some weighting factors and the results are summed up in two frame storages. If the weighting factors in channel 1 approximate a sin- and that in channel 2 a −cos-function, the two frame storages contain the in-phase (0°) and the out-of-phase (−90°) T-modulation signal of the basic harmonic of the heating power signal. Mathematically this correlation procedure is a discrete Fourier transformation of the T-signal, thus the 0° signal represents the real part and the −90° signal the inverse of the imaginary part of the Fourier transform of the basic harmonic of the T signal. The non-inverted imaginary part of the Fourier transform is not used in FA of electronic devices since it is essentially negative. From these two signals the amplitude and the phase signal as well as the 0°/−90° signal can easily be calculated.

Fig. 6 shows a typical set of images, all coming out of one LIT acquisition on an IC without any faults performed at 3 Hz lock-in frequency. Hence, here about 33 frames were used in each lock-in period. At this frequency the thermal diffusion length in silicon is about 3 mm, but all heat sources are laying less than 2 μm below the surface here. Hence, if there are local heat sources in an IC, they can be imaged with a much better spatial resolution than the thermal diffusion length. In addition to the mentioned LIT images always a "topography" image is recorded, which is a single IR image taken before the LIT procedure. While in Fig. 6 the amplitude, the 0°, and the −90° images are all modulated by the emissivity contrast (which also dominates the topography image of the unpowered device), the phase and the 0°/−90° image are free of the emissivity contrast. This is because both of them rely on the ratio of the 0° and the −90° signal, which are both affected by the emissivity in the same way.

4. Results

4.1. Defect localization on decapsulated IC device

A typical result of a LIT investigation of a faulty device is shown in Fig. 7. The encapsulation material of the device was removed by chemical etching (using a solution of 100% fuming nitric acid at an ambient temperature of 35 °C) allowing a direct optical access to

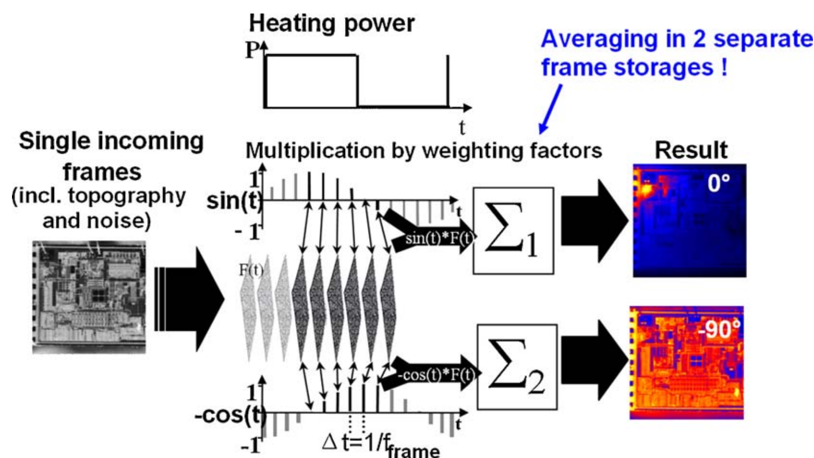

Fig. 5. 2-Channel LIT image correlation procedure.

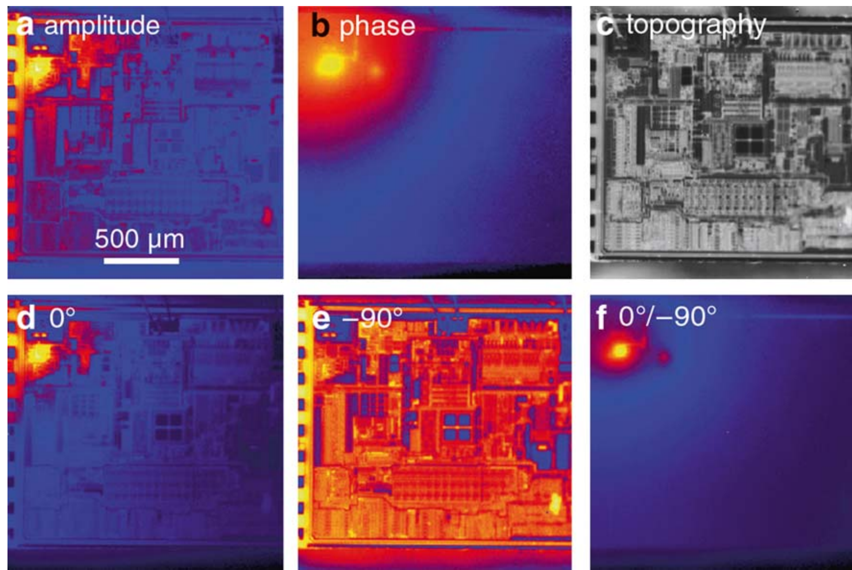

Fig. 6. Different LIT signal representations (f = 3 Hz).

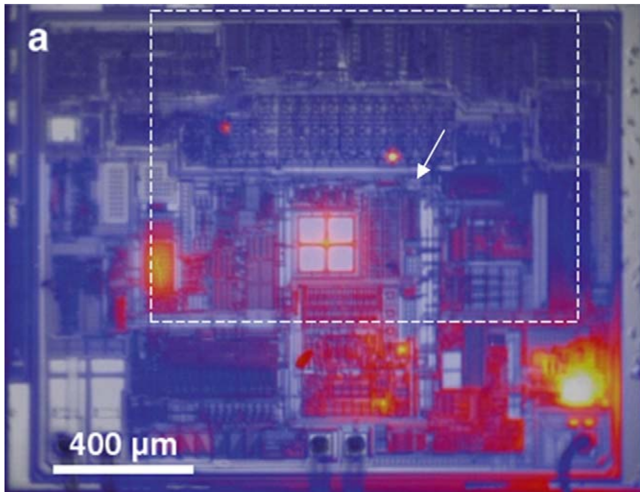

Fig. 7. LIT investigation of a device with a fault (arrow). Superposition of topography and LIT image.

the IC. For this measurement the IC was driven by a pulsed bias of 5 V where 630 μA were flowing, and the lock-in frequency was 25 Hz (4 frames per image). The amplitude of the local temperature modulation in the fault position was in the order of 1 mK. The overlay of the topography image (in grey) and the LIT amplitude image (in colour) is shown. The position of the actual fault is marked by an arrow.

The heat sources are located in the IC structure up to 2 μm below the surface, as usual. The diffraction-limited spatial resolution of LIT can be further improved by applying a so-called solid immersion lens (SIL [13]). This is basically a small hemispherical lens made from silicon, which is placed with its plane side on the surface of the IC and acts as a magnifying glass with a magnification factor of the refraction index of silicon (3.5). Since the defect region is now "immersed" in silicon material, where also the wavelength is reduced by 3.5, the application of a SIL improves the spatial resolution by a factor of 3.5 from about 5 μm to 1.5 μm. The precise localization of the defect site allows a focused ion beam (FIB) preparation of a cross-section specimen for a further scanning electron beam microscope (SEM) investigation, which is shown in Fig. 8. This image shows residues of a TiN barrier layer which was not

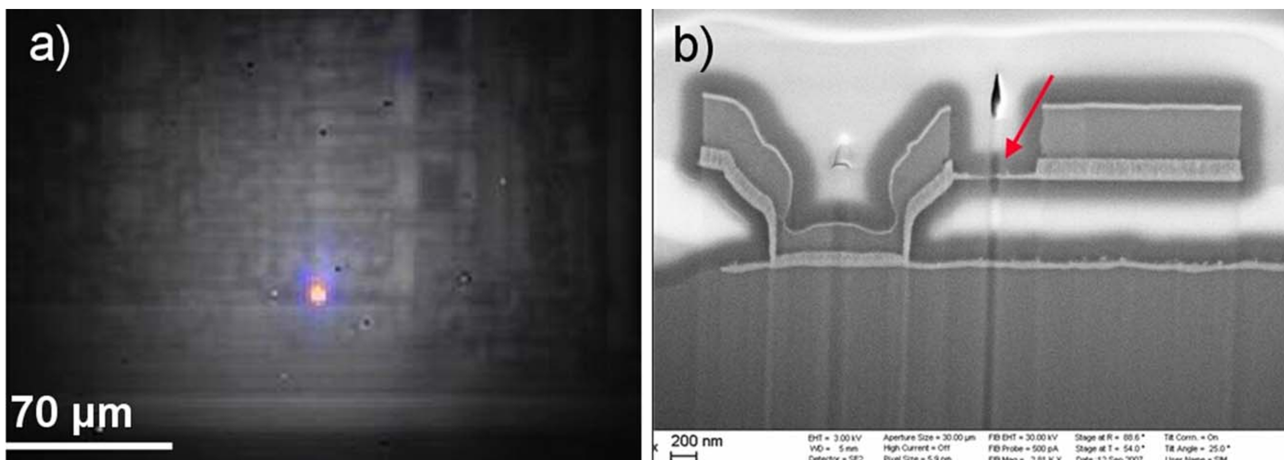

Fig. 8. (a) High magnified image (superposition topography + LIT image) of the defect in Fig. 7 by using a solid immersion lens, (b) SEM image of a cross-section through the defect region.

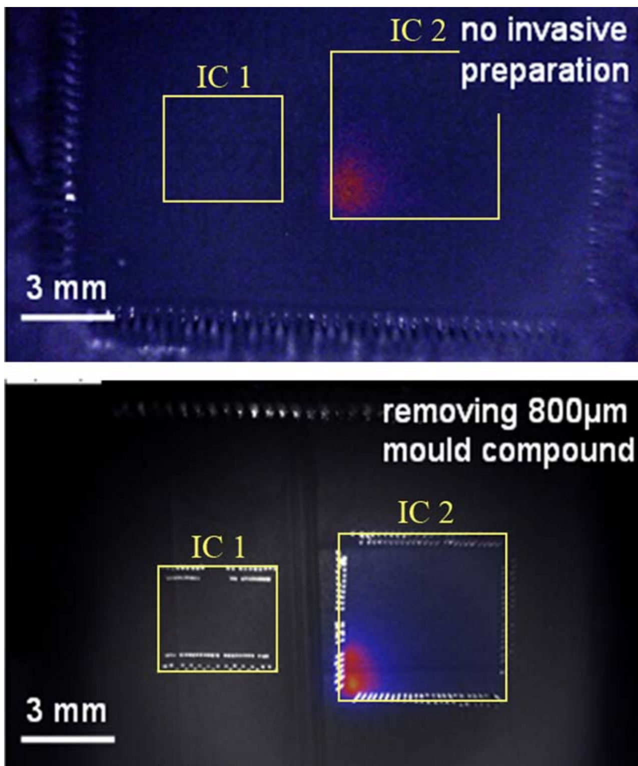

Fig. 9. Upper image: LIT on fully package level shows a thermal emission at the edge of the right chip; lower image: removing 800 μm mould compound by mechanical grinding the hot spot can be allocated on chip level.

completely etched away (arrow) and finally lead to a short between adjacent metal lines.

4.2. Defect localization on fully packaged IC device

As an example for defect localization on fully packaged devices, a defective multi-chip device containing two chips in one package was investigated. The two ICs are placed next to each other inside the package. An electrical short (dissipation power ~ 1 mW) was determined between two pins and the failure site should be localized.

First, LIT was applied at the fully packaged device without any preparation steps in order to separate between chip levels and interconnect level. To enable the heat propagation through the encapsulation material (mould compound, thickness ~800 μm), LIT is performed with low lock-in frequencies. Fig. 9, upper image shows the thermal emission at the device surface. From this first

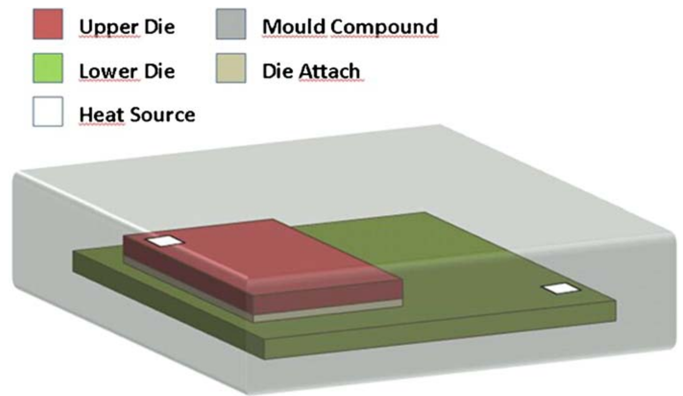

Fig. 11. 3D sketch of the investigated SiP.

measurement in combination with the device design a rough positioning to the edge area of the right chip can be determined. As a next step, the encapsulation material was thinned down to a few tens of micrometers above the upper IC using mechanical grinding which allows an increase of the spatial resolution. LIT was applied for a second measurement, now allocating the defect position clearly to chip level, Fig. 9 lower image.

Determining the defect position most precisely, a third LIT measurement at highest magnification was performed, now with a higher lock-in frequency of 25 Hz, Fig. 10. Because the bond wires were cutted during mechanical grinding the electrical contacting was enabled by local probing of the defect related bond wires. The investigation shows the allocation of the defect on the bonding area.

After the confirmation that the defect was related to the chip structure, it was safe to remove the residual mould compound by chemical etching using a solution of 100% fuming nitric acid at an ambient temperature of 35 °C. Followed SEM investigation and element analysis confirmed an aluminium particle between two bond pads as the short root cause, Fig. 10 right.

4.3. 3D defect localization within a stacked die device

To demonstrate the principle of 3D hot spot localization, a stacked die device containing 2 dies for automotive applications is investigated. A sketch of the internal build up is shown in Fig. 11.

The device contains I/O diode structures on both dies which can be driven as internal heat sources, separately. Heat, coming from these structures has to pass only the covering encapsulation material. Via mechanical cross section, the absolute thickness of the MC layer above the dies is determined, Fig. 12. With knowing the distance to the surface and the thermal properties of the covering material, the theoretical phase shift vs. applied frequency

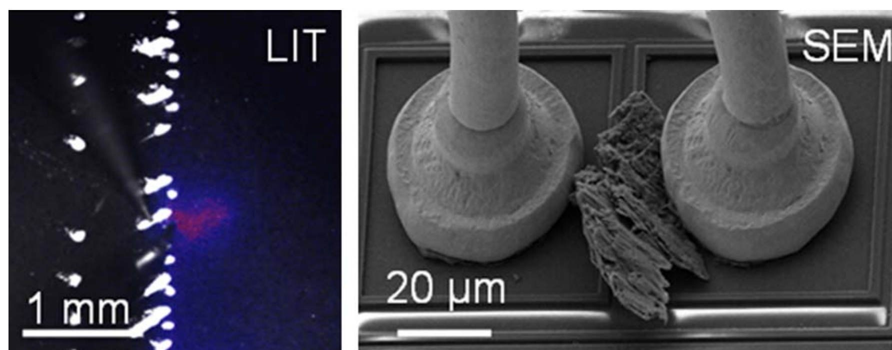

Fig. 10. Detail image of the defective area shows thermal emission on chip level close to the bonding area. SEM on chip level reveals an aluminium particle as short root cause.

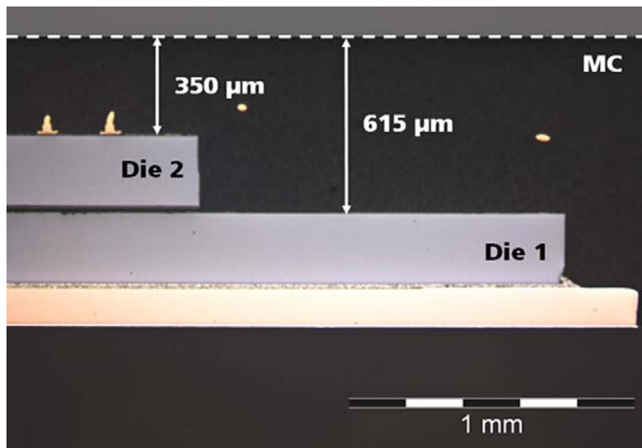

Fig. 12. Sample cross section for defect depth determination.

behaviour for both dies can be calculated.After that, the experimental phase shift is determined using a frequency range from 0.5 to 16 Hz and 1 V. The resulting dissipated power lies at ∼10 mW. Fig. 12 shows a typical phase image (at 10 Hz) for both the lower (a) and the upper die (b).For both dies, the phase shift vs. frequency relationship is determined by measuring the quantitative phase

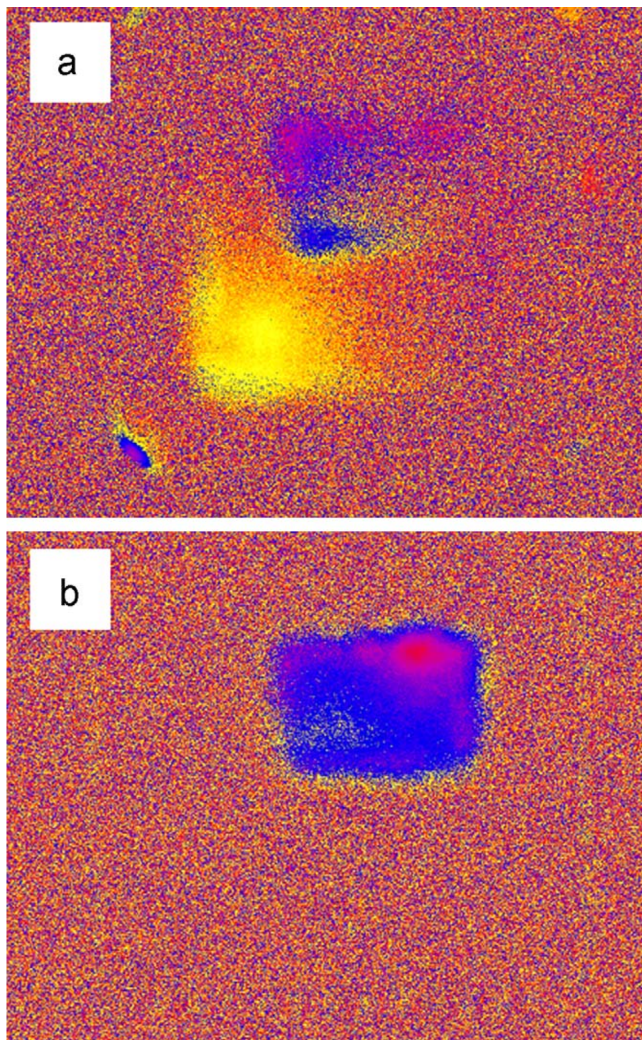

Fig. 13. Resulting phase image at 10 Hz lock-in frequency (a) lower die, (b) upper die.

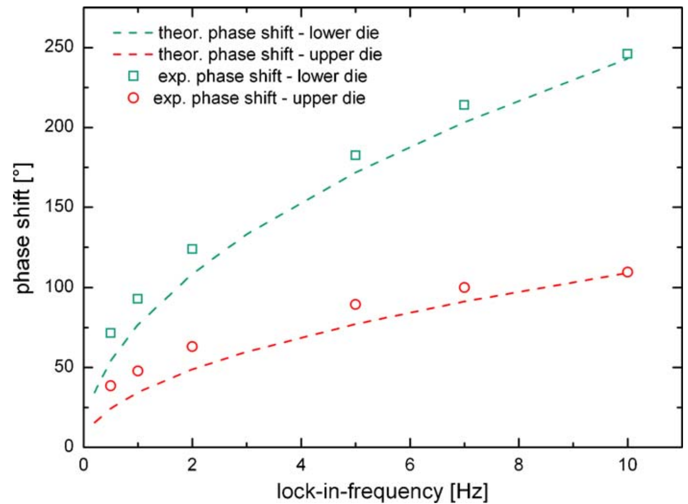

Fig. 14. Comparison of resulting phase shift vs. frequency relationship (dots) compared to theoretical behaviour (dotted lines).

shift value in the centre of the hot spot. The results are plotted and compared to the theoretical behaviour in Fig. 13.

As it can be noticed, a significant difference between lower and upper die phase shift behaviour occurs. Especially at high frequencies and therefore small thermal diffusions lengths, the additional 260 μm MC between upper and lower die result in a phase shift difference up to 150°. Therefore, an identification of the defective die can be done easily. In addition, the experimental results are in good match to the theoretical behaviour. In case of the upper die investigations, a difference between theory and experiment can be regarded which decreases with increasing frequency. Possible reasons for this behaviour could be interactions between IR-transparent (Si) and opaque (MC) material or influences due to a non-perfect heat source geometry. Also, due to the small thickness vs. thermal diffusion length ratio, the occurrence of interference effects could be a possible explanation. Therefore, future experiments should focus on the influence of additional influences to the resulting phase shift, like defect geometry, layer interactions or the lateral defect positions. It should be mentioned that the LIT spot size of heat sources buried under opaque layers is smaller than the thickness of the layer, if this depth exceeds the thermal diffusion length in the material (e.g. for MC ∼ 100 μm at 10 Hz). Nevertheless, multiple spots at the same depth can only be detected separately if the distance between them is higher than the spot size at the surface (see Fig. 14).

5. Conclusions

It has been shown that lock-in thermography (LIT), which was previously used mostly for non-destructive evaluation of buried defects in materials, can be used on a microscopic scale for failure analysis in microelectronic devices. Many electrically defects are connected with weak local heat sources which allows a thermographic localization of the faults. There are also other microthermographic techniques available like liquid crystal microscopy or fluorescent micro thermal imaging. However, the sensitivity limit of these techniques is about a factor 100 worse than that of LIT. Thus, all defects visible in liquid crystal microscopy or fluorescent micro thermal analysis can also easily be detected in LIT, but not all defects visible in LIT can be detected by the conventional techniques due to sensitivity limitations. If a defect-induced local heat source dissipates more that about 10 μW, it can reliably be detected by LIT on IC surface. Of course, for buried defects the detection limit is a function of the defect depth and the applied lock-in frequency.

In the last years lock-in thermography has become an established failure analysis method for microelectronic devices and also for solar cells. The limited spatial resolution of LIT can be improved by applying a solid immersion lens. Furthermore, LIT can be applied as one of only a few methods for fully and non-destructive 3D defect localization on system in package devices. Quantitative phase shift analysis in combination with theoretical heat propagation calculations enabling the identification of defective ICs inside of packaged devices and/or IC stacks. A successful application of 3D LIT on a real device was shown within this paper.

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